MODULE I

OPERATIONAL AMPLIFIERS (OP AMPS)

1.1 INTRODUCTION

The operational amplifier, most commonly referred as 'op-amp' was introduced in 1940s. The first operational amplifier was designed in 1948 using vacuum tubes. In those days, it was used in the analog computers to perform a variety of mathematical operations such as addition, subtraction, multiplication etc. Due to its use in performing mathematical operations it has been given a name operational amplifier. Due to the use of vacuum tubes, the early op-amps were bulky, power consuming and expensive.

Robert J. Widlar at Fairchild brought out the popular 741 integrated circuit (IC) op-amp between 1964 to 1968. The IC version of op-amp uses BJTs and FETs which are fabricated along with the other supporting components, on a single semiconductor chip or ¢ wafer which is of a pinhead size. With the help of IC op-amp, the circuit design becomes very simple. The variety of useful circuits can be built without the necessity of knowing about the complex internal circuitry. Moreover, IC op-amps are inexpensive, take up less space and consume less power. The IC op-amp has become an integral part of almost every electronic circuit which uses linear integrated circuit. The modern linear IC op-amp works at lower voltages. It is so low in cost that millions are now in use, annually.

Because of their low cost, small size, versatility, flexibility, and dependability, op-amps are used in the fields of process control, communications, computers, power and signal sources, displays and measuring systems.

1.2 OP-AMP SYMBOL AND TERMINALS

The symbol for an op-amp along with its various terminals, is shown in the Fig, 1.1. The op-amp is indicated basically by a triangle which points in the direction of the signal flow.

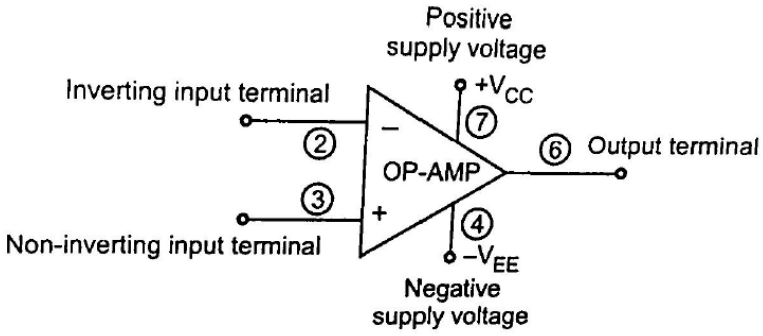


Fig: 1.1 Op-Amp Symbol

All the op-amps have at least following five terminals

- The positive supply voltage terminal Vcc or + V.
- The negative supply voltage terminal - V_{EE} or - V.

- The output terminal.
- The inverting input terminal, marked as negative.
- The noninverting input terminal, marked as positive.

The input at inverting input terminal results in opposite polarity (antiphase) output. While the input at noninverting input terminal results in the same polarity (phase) output. This is shown in the Fig. 1.2 (a) and (b). The input and output are in antiphase means having 180° phase difference in between them while in-phase input and output means having 0° phase difference in between them.

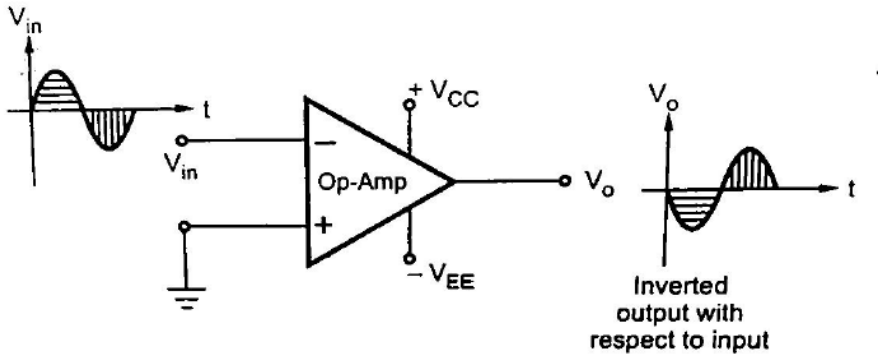


Fig 1.2(a): Input applied to Inverting Terminal

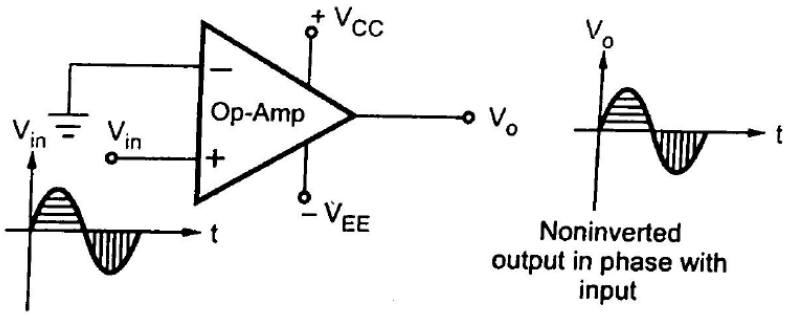


Fig 1.2(b): Input applied to Inverting Terminal

1.3 BLOCK DIAGRAM REPRESENTATION OF OP-AMP

As mentioned earlier, now a days op-amps are available in an integrated circuit form. Commercial integrated circuit op-amps usually consists of four cascaded blocks. The block diagram of IC op-amp is shown in the Fig. 1.3

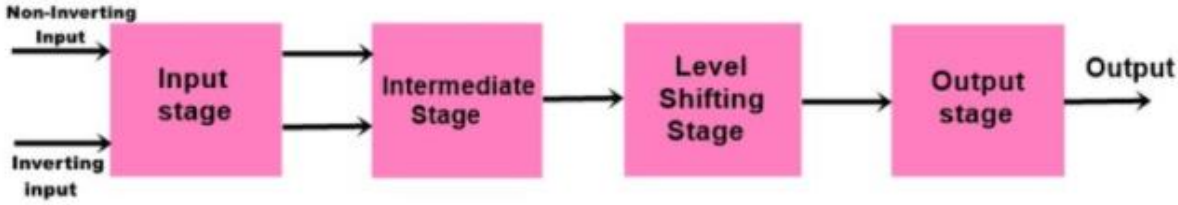


Fig 1.3: Internal Block diagram schematic of Op-Amp

1.3.1 Input Stage

The input stage requires high input impedance to avoid loading on the sources. It requires two input terminals. It also requires low output impedance. All such requirements are achieved by using the dual input, balanced output differential amplifier as the input stage. The function of a differential amplifier is to amplify the difference between the two input signals. The differential amplifier has high input impedance. This stage provides most of the voltage gain of the amplifier.

1.3.2 Intermediate Stage

The output of the input stage drives the next stage which is an intermediate stage. This is another differential amplifier with dual input, unbalanced i.e. single ended output. The overall gain requirement of the op-amp is very high. The input stage alone cannot provide such a high gain. The main function of the intermediate stage is to provide an additional voltage gain required. Practically, the intermediate stage is not a single amplifier but the chain of cascaded amplifiers called multistage amplifiers.

1.3.3 Level Shifting Stage

All the stages are directly coupled to each other. As the op-amp amplifies d.c. signals also, the coupling capacitors are not used to cascade the stages. Hence the d.c. quiescent voltage level of previous stage gets applied as the input to the next stage. Hence stage by stage d.c. level increases well above ground potential. Such a high d.c. voltage level may drive the transistors into saturation. This further may cause distortion in the output due to clipping. This may limit the maximum a.c. output voltage swing without any distortion. Hence before the output stage, it is necessary to bring such a high d.c. voltage level to zero volts with respect to ground.

The level shifter stage brings the d.c. level down to ground potential, when no signal is applied at the input terminals. Then the signal is given to the last stage which is the output stage.

The buffer is usually an emitter follower whose input impedance is very high. This prevents loading of the high gain stage.

1.3.4 Output Stage

The basic requirements of an output stage are low output impedance, large a.c. output voltage swing and high current sourcing and sinking capability. The push-pull complementary amplifier meets all these requirements and hence used as an output stage. This stage increases the output voltage swing and keeps the voltage swing symmetrical with respect to ground. The stage raises the current supplying capability of the op-amp

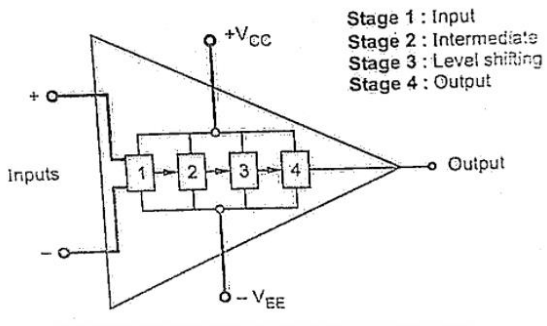


Fig 1.4: Overall Block diagram of an Op-amp

1.4 IDEAL OP-AMP

The ideal op-amp is basically an amplifier which amplifies the difference between the two input signals. In its basic form, the op-amp is nothing but a differential amplifier.

Ideal Op-amp Characteristics

An ideal op-amp has two input signals V_1 and V_2 applied to non-inverting and inverting terminals, respectively.

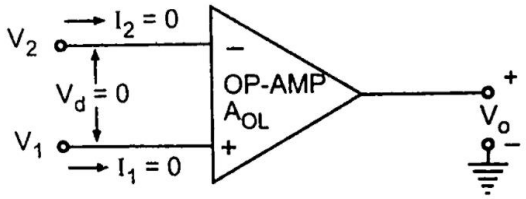


Fig 1.5: Ideal Op-amp

1. An ideal op-amp draws no current at both the input terminals i.e. $I_1 = I_2 = 0$. Thus its input impedance is infinite. Any source can drive it and there is no loading on the driver stage.
2. The gain of an ideal op-amp is infinite (∞), hence the differential input Vd =V_1 - V_2 is essentially zero for the finite output voltage Vo
3. The output voltage Vo is independent of the current drawn from the output terminals. Thus its output impedance is zero and hence output can drive an infinite number of other circuits.

These properties are expressed generally as the characteristics of an ideal op-amp. The various characteristics of an ideal op-amp are:

a) Infinite voltage gain: It is denoted as A_{OL}. It is the differential open loop gain and is infinite for an ideal op-amp.

b) Infinite input impedance : The input impedance is denoted as Rin and is infinite for an ideal op-amp. This ensures that no current can flow into an ideal op-amp.

c) Zero output impedance : The output impedance is denoted as Ro and is zero for an ideal op-amp. This ensures that the output voltage of the op-amp remains same, irrespective of the value of the load resistance connected.

d) Zero offset voltage : The presence of the small output voltage though V1 = V2= 0 is called an offset voltage. It is zero for an ideal op-amp. This ensures zero output for zero input signal voltage.

e) Infinite Bandwidth

The range of frequency over which the amplifier performance is satisfactory is called its bandwidth. The bandwidth of an ideal op-amp is infinite. This means the operating frequency range is from 0 to ∞ . This ensures that the gain of the op-amp will be constant over the frequency range from d.c. (zero frequency) to infinite frequency. So op-amp can amplify d.c. as well as a.c. signals.

f) Infinite CMRR : The ratio of differential gain and common mode gain is defined as CMRR. Thus infinite CMRR of an ideal op-amp ensures zero common mode gain. Due to this common mode noise output voltage is zero for an ideal op-amp.

g) Infinite slew rate: This ensures that the changes in the output voltage occur, simultaneously with the changes in the input voltage. The slew rate is important parameter of op-amp. When the input voltage applied is step type which changes instantaneously then the output also must change rapidly as input changes. If output does not change with the same rate as input then there occurs distortion in the output. Such a distortion is not desirable. ***Infinite slew rate indicates that output changes simultaneously with the changes in the input voltage.***

The parameter slew rate is actually defined as the maximum rate of change of output voltage with time and expressed in V/μs.

$$Slew\ Rate = S = \left.\frac{dV_0}{dt}\right|_{maximum}$$

Slew Rate Equation

Let Vs be the input Voltage & Vo be the output voltage

$$Vs = Vm\ Sin\ \omega t$$

$$Vo = Vm\ Sin\ \omega t(\text{ output of Voltage follower})$$

$$\frac{dVo}{dt} = Vm(\omega cos\omega t)$$

But $\left.\frac{dVo}{dt}\right|_{Max} = Slew\ Rate$, for maximum value of $\frac{dVo}{dt}$, $cos\omega t = 1$;

Therefore $S = \left.\frac{dVo}{dt}\right|_{Max} = \omega Vm$

$$S = 2\pi f V_m \times 10^{-6} \quad V/\mu S$$

h) Power Supply Rejection Ratio (PSRR) :

The power supply rejection ratio is defined as the ratio of the change in input offset voltage due to the change in supply voltage producing it, keeping other power supply voltage constant. It is also called Power Supply Sensitivity.

So if VEE is constant and due to change in Vcc, there is change in input offset voltage then PSRR is expressed as,

$$PSRR = \frac{\Delta V_{ios}}{\Delta V_{CC}}\Big|_{V_{EE}\ constant}$$

if Vcc is constant and due to change in VEE, there is change in input offset voltage then PSRR is expressed as

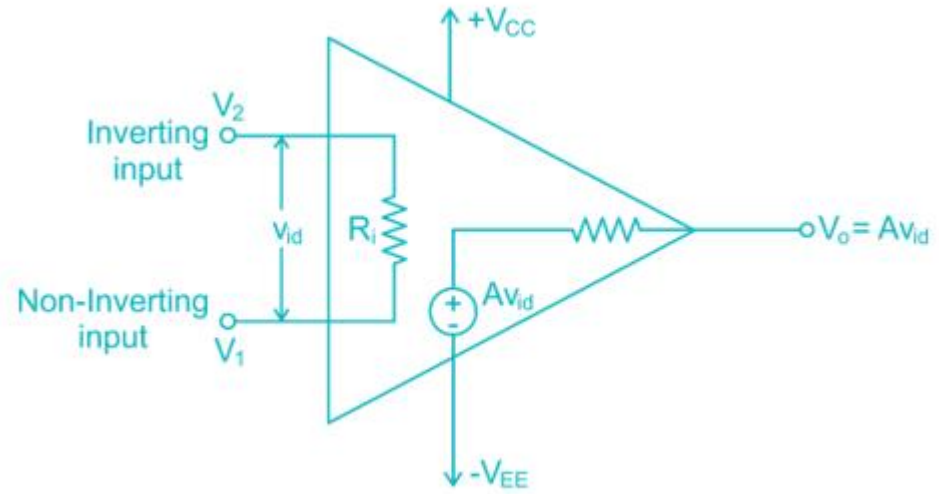
$$PSRR = \frac{\Delta V_{ios}}{\Delta V_{EE}}\Big|_{V_{CC}\ constant}$$

It is expressed in mV/V or μV/V and its ideal value is zero.

Ideal & Practical Characteristics can be summarized as

Characteristics	Symbol	Ideal Parameter Values	741 Parameter Values
Open loop voltage gain	AOL	∞	200000
Input Impedance	Rin	∞	2MΩ
Output Impedance	Ro	0	75Ω
Offset Voltage	Voo	0	2mV-6mV
Bandwidth	B.W	∞	1MHz
CMRR	ρ	∞	90dB
Slew Rate	S	∞	0.5V/μS
Power Supply Rejection Ratio	PSRR	0	150μV/V

1.5 EQUIVALENT CIRCUIT OF OPAMP



- Op-Amp Can be Modelled as Voltage controlled Voltage source (VCVS)
- $AV_{id} - Equivalent\ Thevenian\ Voltage\ source$

- Ro- output Resistance
- Vo= AV_{id}=$A(V_1-V_2)$
- Vid= Difference Voltage between inverting & non inverting Terminals

1.6 OPEN LOOP CONFIGURATIONS

The term open loop indicates 'no connection', either direct or via another network that exists between the output and input terminals. That is, the output signal is not a feedback in any form as part of the input signal.

When connected in open loop configuration, the op-amp simply functions as a high gain amplifier. There are three open loop op-amp configurations:

- Differential amplifier
- Inverting amplifier
- Non-inverting amplifier

1.6.1 Differential amplifier

Fig. shows the open loop differential amplifier in which input signals V_{in1} and V_{in2} are applied to the positive and negative input terminals. Since the op-amp amplifies the difference between the two input signals, this configuration is called the differential amplifier

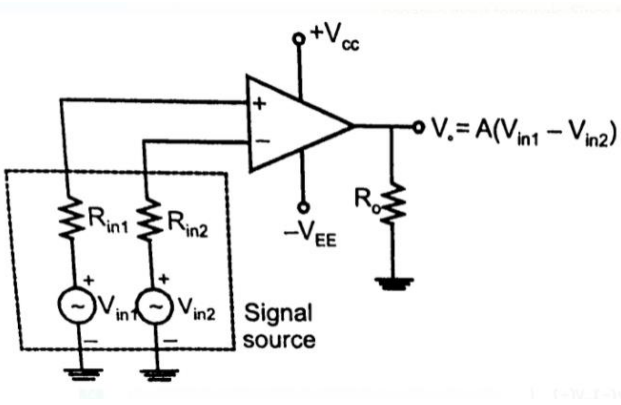


Fig 1.6 : Differential Amplifier using OP-Amp

The op-amp is a versatile device because it amplifies both ac and dc input signals. This means that V_{in1} and V_{in2} could be either ac or dc voltage. The source resistance R_{in1} and R_{in2} are normally negligible compared to the input resistance Ri. Therefore the voltage drop across these resistors can be assumed to be zero, which then implies that $V_1 = V_{in1}$ and $V_2 = V_{in2}$. Substituting these value in equation

$$V_0 = AV_{id} = A(V_1 - V_2)$$

$$V_0 = AV_{id} = A(V_{in1} - V_{in2})$$

1.6.2 Inverting Amplifier

In the inverting amplifier, input voltage is applied in the inverting input terminal. The non- inverting terminal is grounded. Since $V_1 = 0$ and $V_2 = Vin$

$$V_0 = AV_{id} = A(V_1 - V_2)$$

$$V_0 = AV_{id} = -AV_2$$

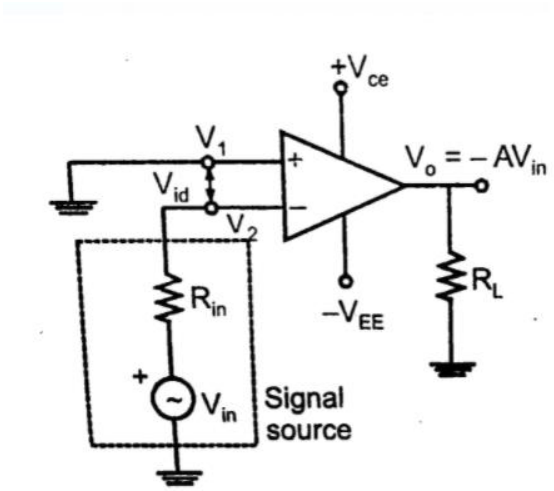


Fig 1.7: Inverting Amplifier

The negative sign indicates that the output voltage is out of phase with respect to input by 180° or is of opposite polarity. Thus in the inverting amplifier the input signal is amplified by gain A and is also inverted at the output

1.6.3 Non inverting amplifier

Fig shows the open loop non-inverting amplifier. In this configuration the input signal is to the non-inverting (positive) input terminal, and the inverting terminal is connected to ground

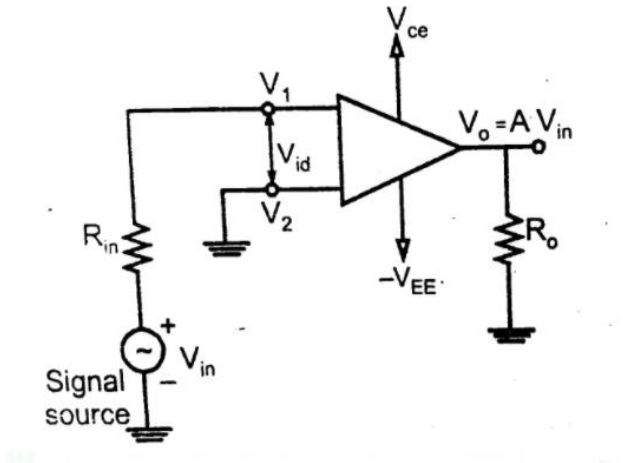


Fig 1.8: Non-Inverting Amplifier

From the circuit $V_1 = V_{in}$ *and* $V_2 = 0$

$$V_0 = A(V_1 - V_2) = AV_1$$

This means that the output voltage is larger than the input voltage by gain A and is in phase with the input signal.

1.7 VOLTAGE TRANSFER CURVE

The ideal op-amp produces the output proportional to the difference between the two input voltages. The graphical representation of this statement gives the voltage transfer curve. It is the graph of output voltage Vo plotted against the difference input voltage Vd, assuming gain constant. This graph is called transfer characteristics of the op-amp.

Now the output voltage is proportional to difference input voltage but only upto the positive and negative saturation voltages of op-amp. These saturation voltages are specified by the manufacturer Vo in terms of output voltage swing rating of an op-amp, for given value of supply voltages .These saturation voltages are slightly less than the supply voltages.

Thus, the voltage transfer curve is a straight line till output reaches saturation voltage level. Thereafter output remains ideal voltage transfer curve is shown in the Fig 1.9

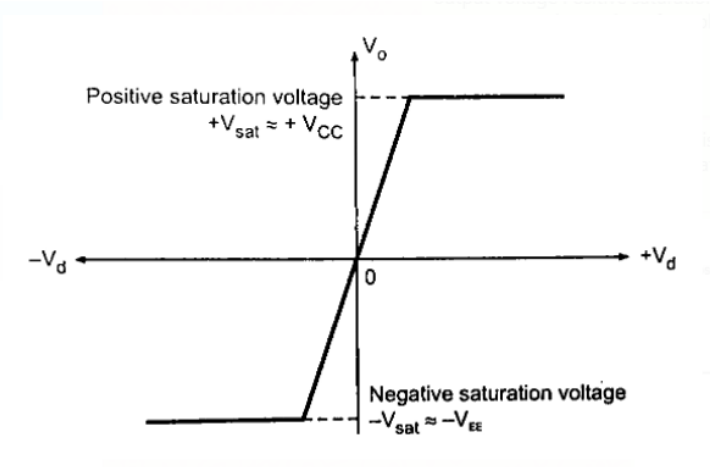


Fig 1.9: Ideal Voltage Transfer Curve

1.8 FREQUENCY RESPONSE CURVE

Ideally, an op-amp should have an infinite bandwidth. This means the gain of op-amp must remain same for all the frequencies from zero to infinite. Till now we have assumed gain of the op-amp as constant but practically op-amp gain decreases at higher frequencies. Such a gain reduction with respect to frequency is called roll off.

This happens because gain of the op-amp depends on the frequency and hence mathematically it is a complex number. Its magnitude and phase changes with frequency.

The plot showing the variations in magnitude and phase angle of the gain due to the change in frequency is called frequency response of the op-amp.

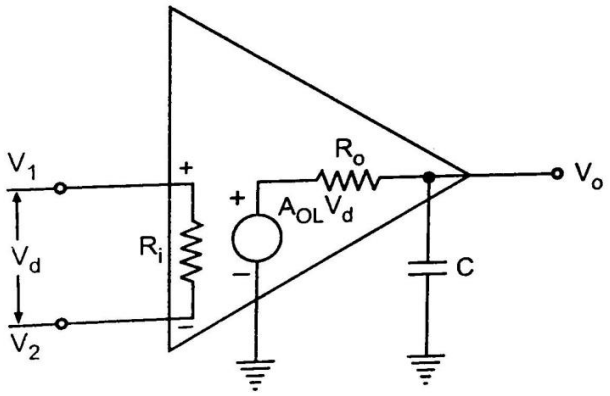


Fig 1.10: High Frequency model of Op-Amp

To obtain the frequency response, consider the high frequency model of the op-amp with a capacitor C at the output, taking into account the capacitive effect present. It is shown in the Fig.1.10 .

Let -jXc be the capacitive reactance due to the capacitor C. From the Fig. 1.10, using voltage divider rule

$$V_0 = A_{OL}V_d \frac{-jX_C}{R_0 - jX_C} \quad ; X_C = 2\pi fC$$

$$V_0 = A_{OL}V_d \times \frac{\frac{1}{j2\pi fC}}{R_0 + \frac{1}{j2\pi fC}} = \frac{A_{OL}V_d}{1 + j2\pi fR_0C}$$

$$A_{OL}(f) = \frac{V_0}{V_d} = \frac{A_{OL}}{1 + j2\pi fR_0C}$$

Let $f_C = \frac{1}{2\pi R_0 C}$= Cut off frequency of Op amp

$$A_{OL}(f) = \frac{V_0}{V_d} = \frac{A_{OL}}{1 + j\frac{f}{f_C}}$$

$$|A_{OL}(f)| = \frac{A_{OL}}{\sqrt{1 + \left(\frac{f}{f_C}\right)^2}}$$

As the frequency increases till f_C the gain is almost constant but after f_C the gain reduces with a rate of -20 dB/decade

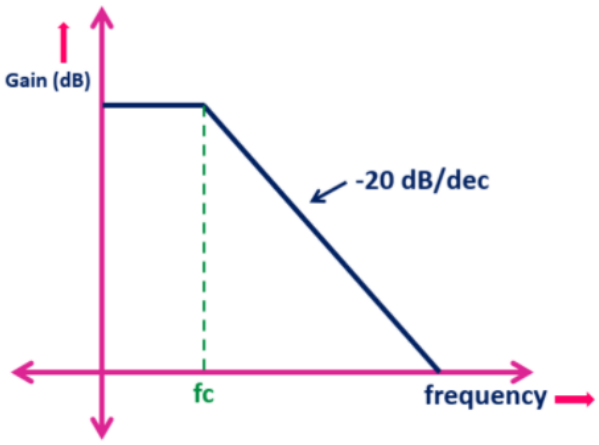


Fig 1.11 Frequency Response of Op-Amp

1.9 DIFFERENTIAL AMPLIFIERS

The Differential Amplifier Amplifies the difference between two input voltage signals. Hence It is called Differential Amplifier.

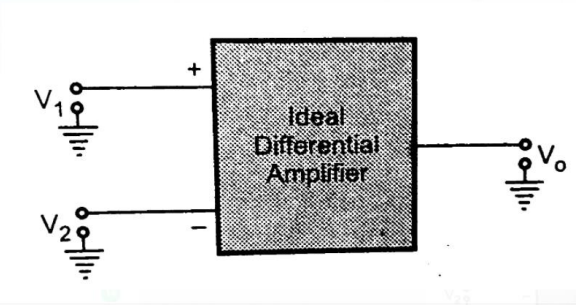


Fig :1.12 Ideal Differential Amplifier

V_1 and V_2 are the two input signals while V_0, is the single ended output. Each signal is measured with respect to the ground. In an ideal differential amplifier, the output voltage V_0, is proportional to the difference between the two input Signals. Hence we can write,

$V_0 = A_d(V_1 - V_2)$-------(1)

$V_0 \propto (V_1 - V_2)$

Differential Gain (Ad)

From Equation 1 we can write $V_0 = A_d(V_1 - V_2)$ where Ad is the gain which differential amplifier amplifies the difference between the two input signals. Hence called Differential Gain

$$V_0 = A_d V_d$$

$$A_d = \frac{V_0}{V_d}$$

Generally Differential Gain is expressed in dB.

$$A_d = 20\log(Ad) \qquad in\ dB$$

Common Mode Gain Ac.

If we apply two input voltages which are equal in all the respects to the differential amplifier i.e. $V_1 = V_2$, then ideally the output voltage $V_0 = (V_1 - V_2)$ Aa must be zero. But the output voltage of the practical differential amplifier not only depends on the difference voltage but also depends on the average common level of the two inputs. Such an average level of the two input signals is called common mode signal denoted as Vc

$$V_C = \frac{V_1 + V_2}{2}$$

The gain with which it amplifies the common mode signal to produce the output is called common mode gain of the differential amplifier denoted as Ac

$$Vo = AcVc$$

$$Ac = \frac{Vo}{Vc}$$

So the Total output of any differential amplifier can be expressed as

$$Vo = AdVd + AcVc$$

Common Mode Rejection Ratio CMRR

When the same voltage is applied to both the inputs, the differential amplifier is said to be operated in a common mode configuration. Many disturbance signals, noise signals _ appear as a common input signal to both the input terminals of the differential amplifier. Such a common signal should be rejected by the differential amplifier

The ability of a differential amplifier to reject a common mode signal is expressed by a ratio called common mode rejection ratio denoted as CMRR. It is defined as the ratio of the differential voltage gain Ad to common mode voltage gain Ac.

$$CMRR = \rho = \left|\frac{Ad}{Ac}\right|$$

Ideally the common mode voltage gain is zero, hence the ideal value of CMRR is infinite. For a practical differential amplifier Ad is large and Ac is small hence the value of CMRR is also very large. Many a times, CMRR is also expressed in dB

$$CMRR\ in\ dB = 20\ log\left|\frac{Ad}{Ac}\right|\ dB$$

The output Voltage can be expressed in terms of CMRR

$$Vo = Advd + AcVc = AdVd\left\{1 + \frac{AcVc}{AdVd}\right\}$$

$$Vo = AdVd\left\{1 + \frac{1}{\left(\frac{Ad}{Ac}\right)} \times \frac{Vc}{Vd}\right\}$$

$$Vo = AdVd\left[1 + \frac{1}{CMRR} \times \frac{Vc}{Vd}\right]$$

Features of Differential Amplifier

The various features of a differential amplifier are

- High differential voltage gain.
- Low common mode gain.
- High CMRR
- Two input terminals.
- High input impedance.
- Large bandwidth.
- Low offset voltages and currents.
- Low output impedance.

1.9.1 TRANSISTORISED DIFFERENTIAL AMPLIFIER

The transistorised differential amplifier basically uses the emitter biased circuits which are identical in characteristics. Such two identical emitter biased circuits are shown in the Fig

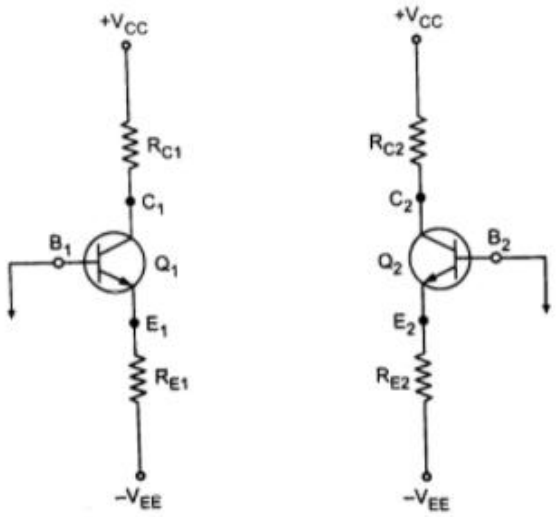


Fig 1.13: Emitter Based Circuits

The two transistors Q_1 and Q_2 have exactly matched characteristics. The two collector resistances R_{c1} and R_{c2} are equal while the two emitter resistances R_{E1} and R_{E2} are also equal.

Thus R_{C1}, = R_{C2} and R_{E1}= R_{E2}

The magnitudes of + Vcc and - V_{EE} are also same. The differential amplifier can be obtained by using such two emitter biased circuits. This is achieved by connecting emitter E_1 of Q_1 to the emitter E_2 of Q_2. Due to this, R_{E1} appears in parallel with R_{E2}, and the combination can be replaced by a single resistance denoted as R_E. The base B_1 of Q_1 is connected to the input 1 which is V_{S1}, while the base B_2 of Q_2 is connected to the input 2 which is V_{s2}. The supply voltages are measured with respect to ground. The balanced output is taken between the collector C_1 of Q_1 and the collector C_2, of Q_2. Such an amplifier is called emitter coupled differential amplifier. The two collector resistances are same hence can be denoted as Rc.

The output can be taken between two collectors or in between one of the two collectors and the ground. When the output is taken between the two collectors, none of them is grounded then it is called balanced output, double ended output or floating output.

When the output is taken between any of the collectors and the ground, it is called unbalanced output or single ended output. The complete circuit diagram of such a basic dual input, balanced output differential amplifier is shown in the Fig.

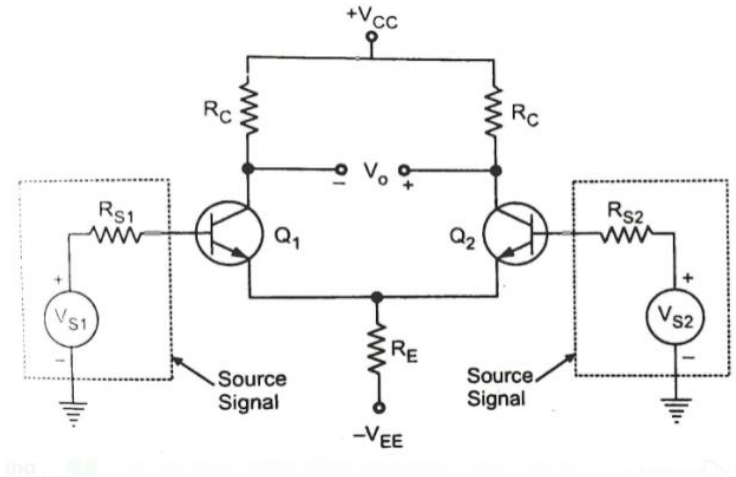


Fig 1.14: Dual input Balanced output Differential Amplifier

As the output is taken between two output terminals, none of them is grounded, it is called balanced output differential amplifier.

Let us study the circuit operation in the two modes namely

- Differential mode operation
- Common mode operation

Differential Mode Operation

In the differential mode, the two input signals are different from each other. Consider the two input signals which are same in magnitude but 180° out of phase. These signals, with opposite phase can be obtained from the center tap transformer. The circuit used in differential mode operation is shown in the Fig.

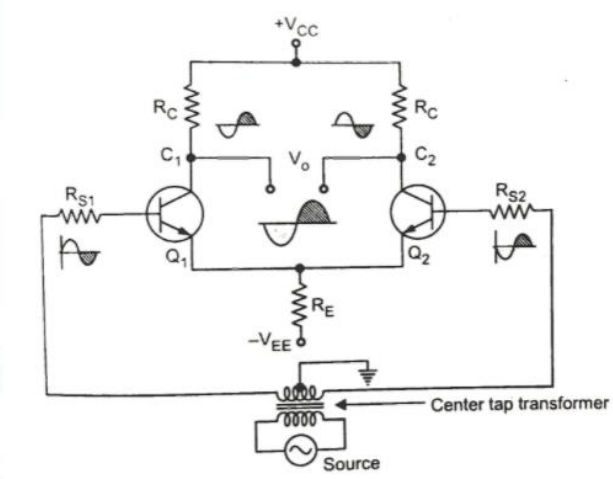


Fig 1.15: Differential Mode Operation

Assume that the sine wave on the base of Q1 is positive going while on the base of Q2 is negative going. With a positive going signal on the base of Q1, an amplified negative going signal develops on the collector of Q1. Due to positive going signal, current through R_E, also increases and hence a positive going wave is developed across R_E. Due to negative going signal on the base of Q2, an amplified positive going signal develops on the collector of Q2. And a negative going signal develops across RE, because of emitter follower action of Q2.

So signal voltages across RE, due to the effect of Q1 and Q2 are equal in magnitude and 180° out of phase, due to matched pair of transistors. Hence these two signals cancel each other and there is no signal across the emitter resistance. Hence there is no a.c. signal current flowing through the emitter resistance. Hence RE in this case does not introduce negative feedback.

While Vo is the output taken across collector of Q1 and collector of Q2. The two outputs on collector 1 and 2 are equal in magnitude but opposite in polarity. And Vo is the difference between these two signals, e.g. +10 - (-10) = + 20. Hence the difference output Vo is twice as large as the signal voltage from either collector to ground.

Common Mode Operation

In this mode, the signals applied to the base of Q1and Q2 are derived from the same source. So the two signals are equal in magnitude as well as in phase. The circuit diagram is shown in fig.

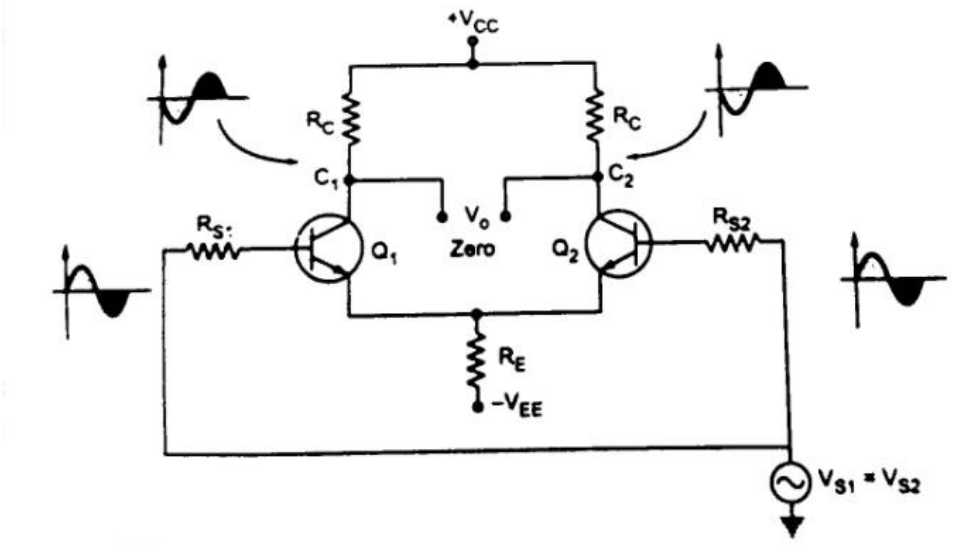


Fig 1.16: Common ode Operation

In phase signal voltages at the bases of Q1 and Q2 causes in phase signal voltages to appear across RE, which add together. Hence RE carries a signal current and provides a negative feedback. This feedback reduces the common mode gain of differential amplifier. While the two signals causes in phase signal voltages of equal magnitude to appear across the two collectors of Q1 and Q2. Now the output voltage is the difference between the two collector voltages, which are equal and also same in phase, e.g. (10) -(10) = 0. Thus the difference output Vo is almost zero, negligibly small. ***Ideally it should be zero.***

Types of Differential Amplifiers

The differential amplifier, in the difference amplifier stage in the op-amp, can be used in four configurations.

- Dual input, balanced output differential amplifier.
- Dual input, unbalanced output differential amplifier
- Single input, balanced output differential amplifier.
- Single input, unbalanced output differential amplifier.

The differential amplifier uses two transistors in common emitter configuration. If output is taken between the two collectors it is called balanced output or double ended output. While if the output is taken between one collector with respect to ground it is called unbalanced output or single ended output. If the signal is given to both the input

terminals it is called dual input, while if the signal is given to only one input terminal and other terminal is grounded it is called single input or single ended input.

Out of these four configurations the dual input, balanced output is the basic differential amplifier configuration. This is shown in the Fig. 1.17 (a). The dual input, unbalanced output differentia: amplifier is shown in the Fig. 1.17 (b). The single input, balanced output differential amplifier is shown in the Fig. 1.17 (c) and the single input, unbalanced output differential amplifier is shown in the Fig. 1.17 (d).

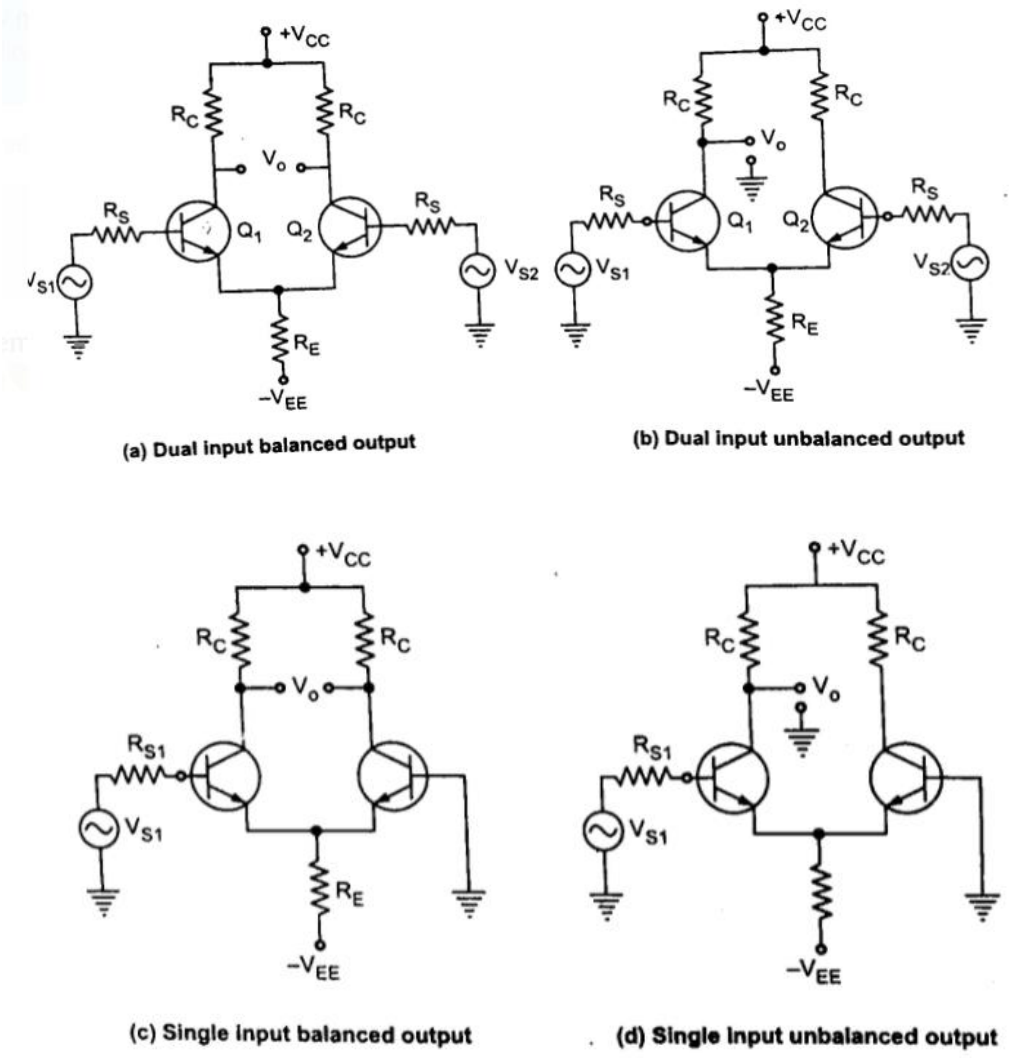


Fig 1.17

The operation of dual input balanced output differential amplifier in differential mode and common mode is already discussed in the last section. This configuration is also called symmetrical differential amplifier.

1.10 D.C. ANALYSIS OF DIFFERENTIAL AMPLIFIER

The d.c. analysis means to obtain the operating point values i.e. I_{CQ} and V_{CEQ} for the transistors used. The supply voltages are d.c. while the input signals are a.c., so d.c. equivalent circuit can be obtained simply by reducing the input a.c. signals to zero. The

d.c. equivalent circuit thus obtained is shown in the Fig. 1.18. Assuming R_{S1}, = R_{S2}, the source resistance is simply denoted by Rs.

The transistors Q_1 and Q_2 are matched transistors and hence for such a matched pair we can assume

- Both the transistors have the same characteristics.
- $R_{E1} = R_{E2}$ hence $R_E = R_{E1} \,||\, R_{E2}$.
- $R_{C1} = R_{C2}$ hence denoted as R_C.
- $|V_{CC}| = |V_{EE}|$ and both are measured with respect to ground.

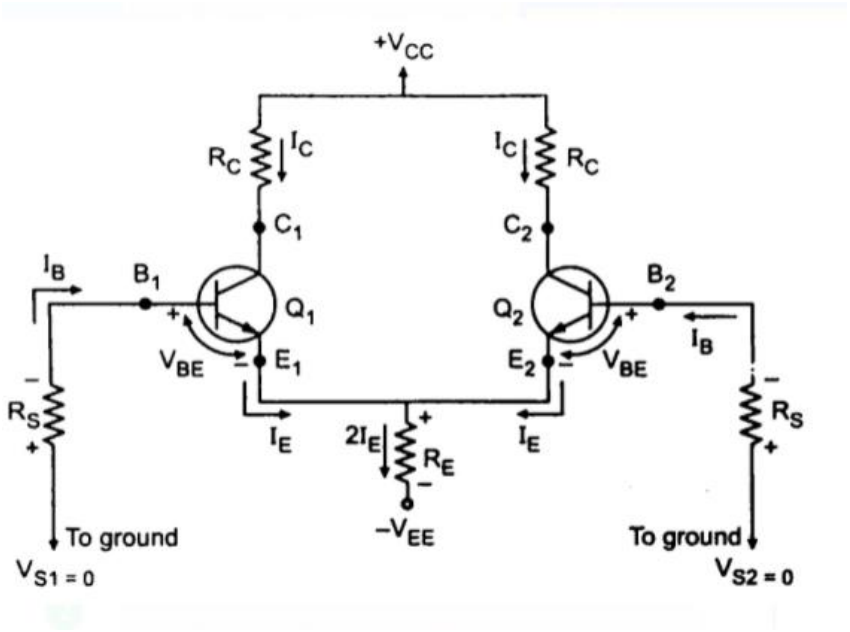


Fig 1.18: DC equivalent Circuit

As the two transistors are matched and circuit is symmetrical, it is enough to find out operating point I_{CQ} and V_{CEQ}, for any one of the two transistors. The same is applicable for the other transistor. Applying KVL to base-emitter loop of the transistor Q_1

$$-I_B R_S - V_{BE} - 2I_E R_E + V_{EE} = 0 \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

But $I_C = \beta I_B \cong I_C \quad ; \; I_B = \frac{I_E}{\beta}$

Therefore Equation (1) becomes

$$\frac{-I_E R_S}{\beta} - V_{EE} - 2I_E R_E + V_{EE} = 0 \ldots\ldots\ldots\ldots\ldots\ldots (2)$$

$$I_E \left[\frac{-R_S}{\beta} - 2R_E\right] + V_{EE} - V_{BE} = 0 \ldots\ldots\ldots\ldots\ldots\ldots (3)$$

$$I_E = \frac{V_{EE} - V_{BE}}{\frac{R_S}{\beta} + 2R_E} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4)$$

Generally $\frac{R_S}{\beta} \ll 2R_E$

$\therefore I_E = \frac{V_{EE}-V_{BE}}{2R_E}$.....(5)

From the equation (5), we can observe that

i) R_E determines the emitter current of Q_1 and Q_2 for the known value of V_{EE}.
ii) The emitter current through Q1 and Q2 is independent of collector resistance R_C.

Now let us determine V_{CE}. As I_E is known and $I_E = I_C$, we can determine the collector voltage of Q_1

$$V_C = V_{CC} - I_C R_C \ldots\ldots (6)$$

Neglecting the drop across Rs, we can say that the voltage at the emitter of Q1 is approximately equal: to $-V_{BB}$. Hence the collector to emitter voltage is

$$\therefore V_{CE} = V_C - V_E = (V_{CC} - I_C R_C) - (-V_{BE})$$

$$\therefore V_{CE} = V_{CC} + V_{BE} - I_C R_C \ldots\ldots\ldots (7)$$

Hence $I_E = I_C = I_{CQ}$ *while* $V_{CE} = V_{CEQ}$ *for given values of* V_{CC} *and* V_{EE}

Key Point: In the equation (5), the sign of V_{EE} is already considered to be negative, while deriving it. Hence while using this equation to solve the problem, only the magnitude of V_{EE} should be used and negative sign of V_{EE} should not be used again.

Thus for both the transistors, we can determine operating point values, using equations (5) and (7). With the same biasing arrangement, the d.c. analysis remains same for all the four possible configurations of differential amplifier

$$I_E = \frac{V_{EE} - V_{BE}}{2R_E} \approx I_{CQ}$$

$$V_{CE} = V_{CC} + V_{BE} - I_{CQ} R_C$$

1.11 A.C. ANALYSIS OF DIFFERENTIAL AMPLIFIER USING H-PARAMETERS

In the a.c. analysis we will calculate the differential gain Ad, common mode gain Ac, input resistance Ri and the output resistance Ro of the differential amplifier circuit, using the h-parameters..

Differential Gain (Ad)

For the differential gain calculation, the two input signals must be different from each other. Let the two a.c. input signals be equal in magnitude but having 180° phase difference in between them. The magnitude of each a.c. input voltage V_{S1} and V_{S2} be Vs /2.

The two a.c. emitter currents $I_{e1}$and I_{e2} are equal in magnitude and 180° out of phase. Hence they cancel each other to get resultant a.c. current through the emitter as zero. Hence for the a.c. purposes emitter terminal can be grounded. The a.c. small signal differential amplifier circuit with grounded emitter terminal is shown in the Fig.1.19

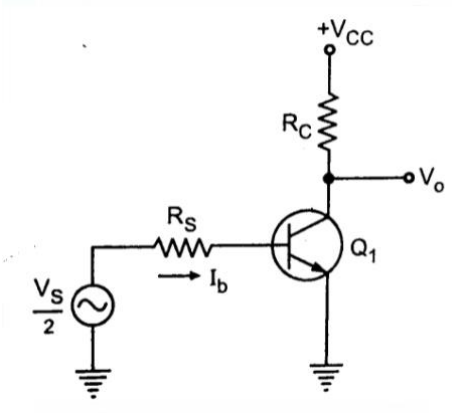


Fig 1.19: AC equivalent circuit for differential operation

As the two transistors are matched, the a.c. equivalent circuit for the other transistor is identical to the one shown in the Fig. 1.19. Thus the circuit can be analysed by considering only one transistor. This is called as half circuit concept of analysis.

The approximate hybrid model for the above circuit can be shown as in the Fig. 1.19, neglecting hoe,

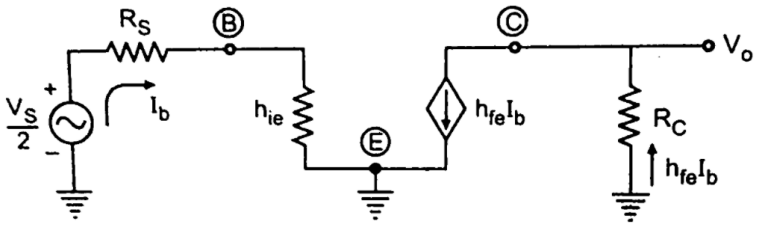


Fig 1.19: Approximate hybrid model

Applying KVL to the input Loop

$$-I_b R_S - I_b h_{ie} + \frac{V_S}{2} = 0 \ldots\ldots\ldots\ldots\ldots (1)$$

$$-I_b(R_S + h_{ie}) = -\frac{V_S}{2}$$

$$I_b = \frac{V_S}{2(R_S + h_{ie})} \ldots\ldots\ldots\ldots (2)$$

Applying KVL to output Loop

$$V_0 = -h_{fe} I_b R_C \ldots\ldots (3)$$

Sub eqn (2) in (3)

$$V_0 = -h_{fe} \frac{V_S}{2(R_S + h_{ie})} R_C$$

$$\frac{V_0}{V_S} = \frac{-h_{fe} R_C}{2(R_S + h_{ie})} \ldots\ldots\ldots (4)$$

The negative sign indicates the phase difference between input and output. Now two input signal magnitudes are $\frac{V_S}{2}$ but they are opposite in polarity, as 180° out of phase.

$$\therefore V_d = V_1 - V_2 = \frac{V_S}{2} - \left(-\frac{V_S}{2}\right) = V_S$$

The magnitude of the Differential gain Ad is

$$A_d = \frac{V_0}{V_S} = \frac{-h_{fe} R_C}{2(R_S + h_{ie})} \ldots\ldots\ldots (5)$$

What we are interested is to obtain Ad for the differential amplifier with the balanced output. Balanced output is across the two collectors of the transistors Q1 and Q2, which are perfectly matched. Such balanced output is double than that obtained above, with unbalanced output. Hence the-expression for Ad with balanced output changes as

$$A_d = 2 \times \frac{-h_{fe} R_C}{2(R_S + h_{ie})}$$

$$A_d = \frac{V_0}{V_S} = \frac{h_{fe} R_C}{(R_S + h_{ie})} \ (Magnitide) \ldots\ldots\ldots (6)$$

This is the Differential Gain for Dual input Balanced output Differential Amplifier Circuit.

Common Mode Gain (Ac)

Let the magnitude of both the a.c. input signals be Vs and are in phase with each other. Hence the differential input Va = 0 while the common mode input Vc is the average value of the two

$$\therefore V_C = \frac{V_1 + V_2}{2} = \frac{V_S + V_S}{2} = V_S \ldots\ldots (7)$$

While the output can be expressed as

$$V_0 = A_C V_S \ldots\ldots (8)$$

$$A_C = \frac{Vo}{Vs} \ldots (9)$$

But now both the emitter currents $I_{e1} = I_{e2} = Ie$, flows through R_E in the same direction. Hence the total current flowing through R_E is 2Ie.

As the two transistors are matched, ac. equivalent of common mode operation can be shown, considering only one transistor, as in the Fig. 1.20 operation can

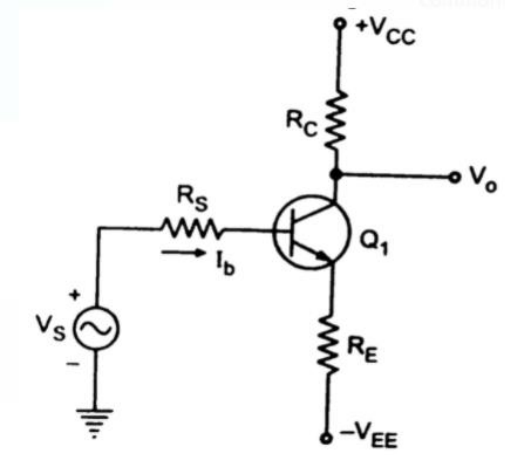


Fig 1.20: AC equivalent circuit for Common mode operation

The approximate hybrid model is

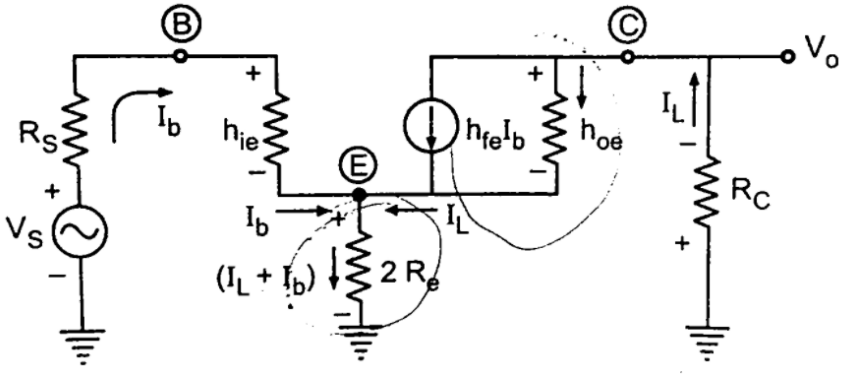


Fig 1.21: approximate hybrid model

As the current through R_E is 2Ie, for simplicity of derivation the current can be assumed to be Ie, and effective emitter resistance as 2 R_e. Hence the emitter resistance is shown 2 R_e in the Fig. 1.21.

So current through Re = load current I_L

effective emitter resistance = 2 Re

current through emitter resistance = I_L+I_b

$$\text{current through hoe} = (I_L - h_{fe}I_b)$$

Applying KVL to the input side,

$$-I_b R_S - I_b h_{ie} - 2R_e(I_L + I_b) + V_S = 0$$

$$V_S = I_b(R_S + h_{ie} + 2R_e) + I_L(2R_e) \ldots\ldots(10)$$

While $V_0 = -I_L R_C$.....(11)

Applying KVL in output loop

$$\frac{-(I_L - h_{fe} I_b)}{h_{oe}} - 2R_e(I_L + I_b) - I_L R_C = 0$$

$$\frac{-I_L}{h_{oe}} + \frac{h_{fe}}{h_{oe}} I_b - 2R_e I_L - 2R_e I_b - I_L R_C = 0$$

$$I_b\left[\frac{h_{fe}}{h_{oe}} - 2R_e\right] = I_L\left[\frac{1}{h_{oe}} + 2R_e + R_C\right]$$

$$I_b\left(h_{fe} - 2R_e h_{oe}\right) = I_L[1 + h_{oe}(2R_e + R_C]$$

$$\therefore \frac{I_L}{I_b} = \frac{\left(h_{fe} - 2R_e h_{oe}\right)}{[1 + h_{oe}(2R_e + R_C]}$$

$$I_b = \frac{I_L[1 + h_{oe}(2R_e + R_C]}{\left(h_{fe} - 2R_e h_{oe}\right)} \ldots\ldots\ldots(12)$$

Substitute the Value of Ib in equation (10)

$$V_S = \frac{I_L[1 + h_{oe}(2R_e + R_C]}{\left(h_{fe} - 2R_e h_{oe}\right)}(R_S + h_{ie} + 2R_e) + I_L(2R_e)$$

$$\frac{V_S}{I_L} = \frac{[1 + h_{oe}(2R_e + R_C]}{\left(h_{fe} - 2R_e h_{oe}\right)}(R_S + h_{ie} + 2R_e) + (2R_e)$$

$$\frac{V_S}{I_L} = \frac{[1 + h_{oe}2R_e + h_{oe}R_C] + (R_S + h_{ie} + 2R_e) + (2R_e)\left(h_{fe} - 2R_e h_{oe}\right)}{\left(h_{fe} - 2R_e h_{oe}\right)}$$

$$= \frac{R_s(1 + 2R_e h_{oe}) + R_s R_c h_{oe} + h_{ie}(1 + 2R_e h_{oe}) + h_{ie} h_{oe} R_C + 2R_e[1 + h_{oe}2R_e + h_{oe}R_C] + (2R_e)\left(h_{fe} - 2R_e h_{oe}\right)}{\left(h_{fe} - 2R_e h_{oe}\right)}$$

$$= \frac{R_s(1 + 2R_e h_{oe}) + R_s R_c h_{oe} + h_{ie}(1 + 2R_e h_{oe}) + h_{ie} h_{oe} R_C + 2R_e + 4{R_e}^2 h_{oe} + 2R_e h_{oe} R_C + 2R_e h_{fe} - 4{R_e}^2 h_{oe}}{\left(h_{fe} - 2R_e h_{oe}\right)}$$

$$= \frac{R_s(1+2R_eh_{oe}) + R_sR_ch_{oe} + h_{ie}(1+2R_eh_{oe}) + h_{ie}h_{oe}R_C + 2R_e + 2R_eh_{oe}R_C + 2R_eh_{fe}}{(h_{fe} - 2R_eh_{oe})}$$

$$= \frac{R_s(1+2R_eh_{oe}) + 2R_e(1+h_{fe}) + h_{ie}(1+2R_eh_{oe}) + h_{oe}R_C(2R_e + R_s + h_{ie})}{(h_{fe} - 2R_eh_{oe})}$$

$$= \frac{2R_e(1+h_{fe}) + (R_s + h_{ie})(1+2R_eh_{oe}) + h_{oe}R_C(2R_e + R_s + h_{ie})}{(h_{fe} - 2R_eh_{oe})}$$

Neglecting the terms of $h_{oe}R_C$ as practically $h_{oe}R_C \ll 1$

$$\frac{V_S}{I_L} = \frac{2R_e(1+h_{fe}) + (R_s + h_{ie})(1+2R_eh_{oe})}{(h_{fe} - 2R_eh_{oe})}$$

$$I_L = \frac{V_S(h_{fe} - 2R_eh_{oe})}{2R_e(1+h_{fe}) + (R_S + h_{ie})(1+2R_eh_{oe})}$$

Substituting the Value of I_L in Equation (11)

$$V_0 = \frac{-V_S(h_{fe} - 2R_eh_{oe})R_C}{2R_e(1+h_{fe}) + (R_S + h_{ie})(1+2R_eh_{oe})}$$

Hence the Common mode gain can be written by neglecting the terms of h_{oe}

$$A_c = \frac{V_0}{V_S} = \frac{-h_{fe}R_C}{2R_e(1+h_{fe}) + (R_S + h_{ie})} \ldots\ldots(13)$$

Common Mode Rejection Ratio(CMRR)

Once the Ad & Ac are obtained ,the expression for CMRR can be obtained as

$$CMRR = \left|\frac{A_d}{A_c}\right| \ldots\ldots(14)$$

$$CMRR = \frac{2R_e(1+h_{fe}) + (R_S + h_{ie})}{(R_S + h_{ie})} \ldots\ldots(15)$$

Differential Input Resistance (Ri)

It is the equivalent resistance between one of the input and the ground when the other input terminal is grounded.

$$R_i = \frac{V_S}{I_b} \ldots\ldots(16)$$

Sub eqn (2) in (16)

$$R_i = \frac{V_S}{\frac{V_S}{2(R_S + h_{ie})}}$$

$$R_i = 2(R_S + h_{ie}) \dots \dots .. (17)$$

Output Resistance (Ro)

It is defined as the equivalent resistance between one of the output terminals with respect to ground. As seen from the Fig. 1.19, the resistance between output terminal with respect to ground is Rc.

$$R_0 = R_C \dots \dots \dots (18)$$

1.12 METHODS OF IMPROVING CMRR

Higher the value of CMRR, better is the performance of differential amplifier. Hence in practice the efforts are always to improve the CMRR of the differential amplifier. Along with the basic circuit, various other circuits are used to improve the performance of differential amplifier.

EFFECT OF R_E

To improve the CMRR, the common mode gain Ac, must be reduced. The common mode gain Ac. approaches zero as R_E tends to infinity. This is because R_E introduces a negative feedback in the common mode operation which reduces the common mode gain Ac. Thus higher the value of R_E, lesser is the value of Ac, and higher is the value of CMRR. The differential gain Ad is not dependent on R_E. But practically R_E can not be selected very high due to certain limitations such as

1. Large Re needs higher biasing voltage to set the operating Q point of the transistors.

2. This increases the overall chip area.

Hence practically instead of increasing R_E various other methods are used which Provide effect of increased R_E without any limitations. Such two methods are

- Constant current bias method.
- Use of current mirror circuit.

Differential Amplifier with Constant Current Source

Without physically increasing the value of R_E, the R_E is replaced by a transistor Operated at a constant current. Such a constant current source circuit gives the effect of a very high resistance without affecting the Q point values of the differential amplifier. The

differential amplifier using constant current bias circuit instead of R_E is shown in figure 1.22.

The transistor used is Q3 and the values of R1, R2 and R3 are selected so as to give the same operating point values for the two transistors Q1 and Q2.

Circuit Analysis

Let current through R3 be I_{E3}; while current through R_1 is I. Neglecting the base current of Q3 which is very small due to large β_{ac}, we can assume that current through R_2 is also I.

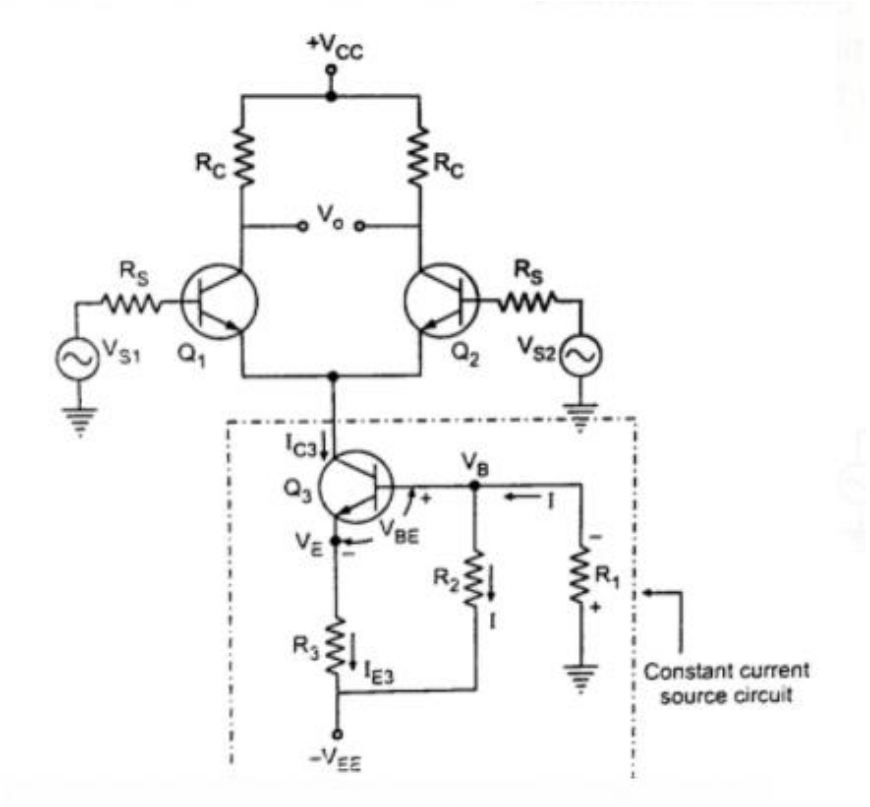


Fig 1.22 : Use of constant current source

Applying Kirchhoff's law

$$-IR_1 - IR_2 + V_{EE} = 0$$

$$I = \frac{V_{EE}}{R_1 + R_2}$$

Now $V_B = -IR_1$

$$V_B = -\frac{V_{EE}}{R_1 + R_2} R_1$$

Now $V_E = V_B - V_{BE}$

$$I_{E3} = \frac{V_E - (-V_{EE})}{R_3}$$

Substitute the values for V_B & V_E

$$I_{E3} = \frac{\frac{-V_{EE}}{R_1 + R_2} R_1 - V_{BE} + (V_{EE})}{R_3}$$

$$I_{E3} = \frac{V_{EE}\left[\frac{R_2}{R_1 + R_2}\right] - V_{BE}}{R_3}$$

Neglecting I_{B3} we can write

$$I_{C3} = I_{E3}$$

Thus as V_{EE}, R1, R2, R3 and V_{BE} are constants, current I_{C3} is almost equal to I_{E3}, and also constant. Thus circuit with transistor Q3, acts as a constant current source

Constant current Bias using Zener

The problem of temperature dependent characteristics of the transistor can be solved by using zener diode. This is because zeners are available over a wide range of voltages and can have a matching temperature coefficient of voltage to those of transistors. Constant current bias circuit using zener is shown

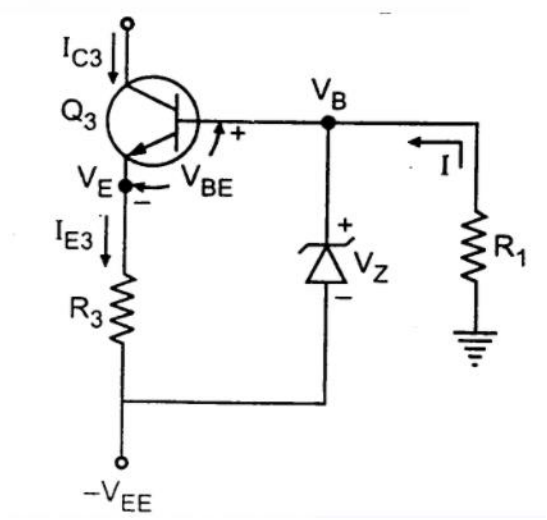


Fig 1.23: Constant current bias using Zener

Circuit Analysis

The Voltage at the base of transistor Q3

$$V_B = -V_{EE} + V_Z$$

$$V_E = V_B - V_{BE}$$

$$V_E = -V_{EE} + V_Z - V_{BE}$$

$$I_{E3} = \frac{V_E - (-V_{EE})}{R_3}$$

$$I_{E3} = \frac{-V_{EE} + V_Z - V_{BE} + V_{EE}}{R_3}$$

$$I_{E3} = \frac{V_Z - V_{BE}}{R_3}$$

While the value of R1 is selected in such a way that zener diode always conducts in reverse region,it can be calculated as

$$R_1 = \frac{V_{EE} - V_Z}{I}$$

The common mode gain is almost zero, providing very large value of CMRR, with a constant current bias. To offer extremely large resistance under a.c. conditions, a simple circuit of constant current source, with less number of components is now a days used. This circuit is called ***current mirror*** or ***current repeater circuit***

CURRENT MIRROR CIRCUIT

The circuit in which the output current is forced to equal the input current is called as current mirror circuit. In a current mirror circuit, the output current is the mirror image of input current. The current mirror circuit is often referred to a **Current Controlled Current Source or CCCS**.

In figure Q3 & Q4 are perfectly matched,

$$V_{BE3} = V_{BE4}\ and\ I_{B3} = I_{B4}\ \ ,I_{C3} = I_{C4}$$

Applying KCL at Node X

$I_2 = I + I_{C4}$.....(1)

Applying KCL at Node Y

$$I = I_{B3} + I_{B4}\ \ .....(2)$$

Note that

$$I_{B3} = I_{B4}$$
$$I_{C3} = I_{C4}$$

$$I = 2I_{B3} = 2I_{B4}\ .....(3)$$

Substitute equation (3) in equation (1)

$$I_2 = 2I_{B4} + I_{C4} = 2I_{B3} + I_{C3}$$

$$\text{Now}\ \ I_{B3} = \frac{I_{C3}}{\beta}$$

$$I_2 = 2\frac{I_{C3}}{\beta} + I_{C3}$$

$$I_2 = \left[\frac{2}{\beta} + 1\right] I_{C3}$$

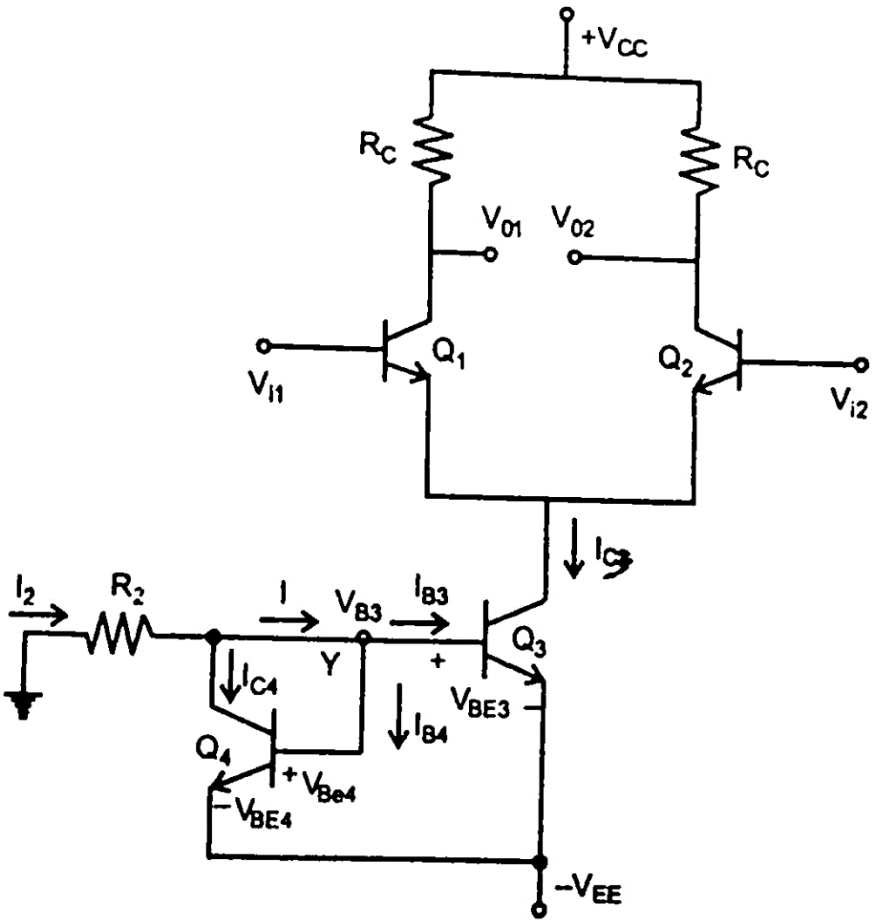


Fig 1.24 : Current Mirror Circuit

Generally β *is very large* $\therefore$ $\frac{2}{\beta}$ *is negligibly small*

$$I_2 \cong I_{C3}$$

Thus Collector current of Q_3 is nearly equal to the current I_2

I_2 can be obtained by applying KVL for the base emitter loop of transistor Q_3

$$-I_2R_2 - V_{BE3} - V_{EE} = 0$$

$$I_2R_2 = V_{EE} - V_{BE3}$$

$$I_2 = \frac{V_{EE} - V_{BE3}}{R_2}$$

By selecting R_2, appropriate I_2 can be set for current mirror circuit

Wilson Current Source Circuit

Another widely used current source using current mirror technique is Wilson current source. High output resistance is the feature of Wilson current source. The Wilson current source circuit is shown in the Fig. 1.25.

The high output resistance is achieved due to the negative feedback through Q3. It also provides base currents cancellation making ***I***, nearly equal to ***I_{ref}***

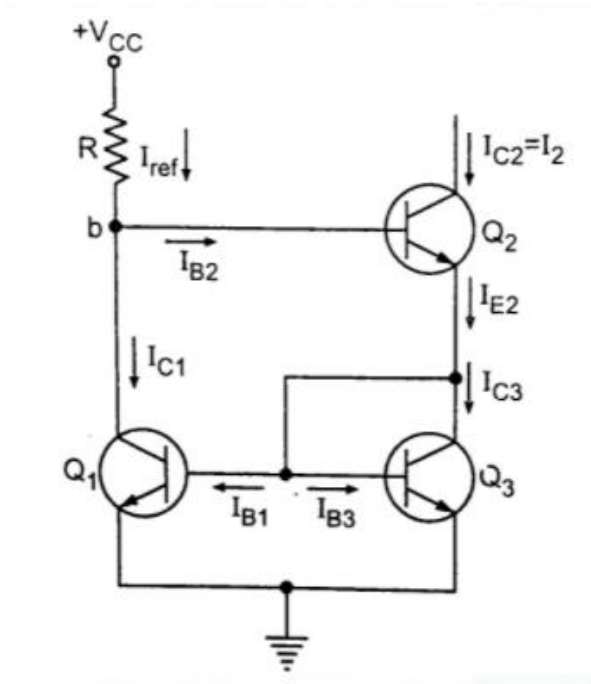


Fig 1.25: ***Wilson Current Source Circuit***

Applying KCL at node b,

$$I_{ref} = I_{C1} + I_{B2} \ldots\ldots (1)$$

$$I_{E2} = I_{C3} + I_{B1} + I_{B3} \ldots\ldots (2)$$

$$\because \; I_{B1} = I_{B2} = I_{B3} = I_B$$

$$I_{E2} = I_{C3} + 2I_B \ldots\ldots (3)$$

$Also\ I_{E2} = I_{C2} + I_{B2}$ also $I_{E2} = I_{C2} + I_B \ldots\ldots\ldots (4)$

$$I_{C2} = I_{E2} - I_B$$

$$I_{C2} = I_{C3} + 2I_B - I_B = I_{C3} + I_B \ldots\ldots\ldots (5)$$

$$I_{C2} = I_{C1}\ as\ all\ transistors\ are\ equal$$

$$\therefore I_{C2} = I_{C1} + I_B \ldots\ldots (6)$$

From equation (1) $I_{ref} = I_{C1} + I_B \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (7)$

Comparing Eqns (6) and (7) We can say

$$I_2 = I_{ref} = I_{C2} \ldots\ldots\ldots\ldots\ldots\ldots (8)$$

Now $I_{E2} = I_{C3} + 2I_B$; $But\ I_B = \frac{I_{C3}}{\beta}$

$$I_{E2} = I_{C3} + 2\frac{I_{C3}}{\beta}$$

$$I_{E2} = I_{C3}\left(1 + \frac{2}{\beta}\right) \quad \ldots\ldots (9)$$

From Equation (4) $I_{E2} = I_{C2} + I_B = I_{C2} + \frac{I_{C2}}{\beta} = I_{C2}\left(1 + \frac{1}{\beta}\right) = \left(\frac{1+\beta}{\beta}\right)$

$$I_{C2} = I_{E2}\left(\frac{\beta}{1+\beta}\right) \ldots\ldots (10)$$

Substitute equation (9) in (10)

$$I_{C2} = I_{C3}\left(1 + \frac{2}{\beta}\right)\left(\frac{\beta}{1+\beta}\right)$$

$$I_{C3} = \frac{I_{C2}}{\left(1 + \frac{2}{\beta}\right)\left(\frac{\beta}{1+\beta}\right)} \ldots\ldots\ldots (11)$$

From equation (1) $I_{ref} = I_{C1} + I_{B2}$

$$I_{C1} = I_{ref} - I_B$$

$$I_{C1} = I_{ref} - \frac{I_{C2}}{\beta} \ldots\ldots\ldots\ldots (12)$$

Since Transistors are identical $I_{C3} = I_{C1}$

$$\therefore Compairing\ Equations\ (11) and\ (12)$$

$$\frac{I_{C2}}{\left(1 + \frac{2}{\beta}\right)\left(\frac{\beta}{1+\beta}\right)} = I_{ref} - \frac{I_{C2}}{\beta}$$

By solving we get

$$I_{C2}\left(\frac{\beta^2+2\beta+2}{\beta(2+\beta)}\right)=I_{ref}$$

$$I_{C2}=I_{ref}\left(\frac{\beta(2+\beta)}{\beta^2+2\beta+2}\right)=I_{ref}\left(\frac{(\beta^2+2\beta+2-2)}{\beta^2+2\beta+2}\right)$$

$$I_{C2}=I_{ref}\left(1-\frac{2}{\beta^2+2\beta+2}\right)$$

The equation shows that the output current I_{C2} and I_{ref} differ by only a factor which is in the order of $\frac{2}{\beta^2}$.

Widlar Current Source

In operational amplifier low input current is required. Hence input stage is biased at very low current, typically at a collector current of the order of 5 μA. Currents of such low magnitude can be obtained with a modified circuit called Widlar current source. The circuit is shown in the Fig 1.26

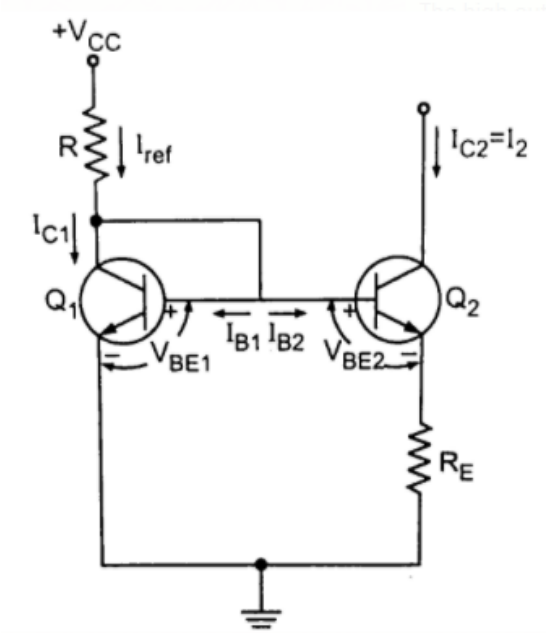


Fig 1.26: Widlar Current Source

The two transistors are identical to each other, but due to emitter resistance R_E, V_{BE1} & V_{BE2} are different. In fact $V_{BE2} < V_{BE1}$ *and hence* $I_{C2} < I_{C1}$ .Due to asymmetric nature of the base emitter loop, the circuits is called "**lens**" rather than a "**mirror**"

Applying KVL in Base emitter loop,

$$V_{BE1}=V_{BE2}+(I_{B2}+I_{C2})R_E \ldots\ldots(1)$$

$$V_{BE1}-V_{BE2}=(I_{B2}+I_{C2})R_E \ldots\ldots(2)$$

For the transistor we can write

$$I_{C1} = I_S \times e^{\frac{V_{BE1}}{V_T}}$$

$$I_{C2} = I_S \times e^{\frac{V_{BE2}}{V_T}}$$

$$\frac{I_{C1}}{I_{C2}} = \frac{I_S \times e^{\frac{V_{BE1}}{V_T}}}{I_S \times e^{\frac{V_{BE2}}{V_T}}} = e^{\left(\frac{V_{BE1}-V_{BE2}}{V_T}\right)}$$

By taking natural log on both sides

$$ln\left(\frac{I_{C1}}{I_{C2}}\right) = \frac{V_{BE1} - V_{BE2}}{V_T}$$

$$V_{BE1} - V_{BE2} = ln\left(\frac{I_{C1}}{I_{C2}}\right) \times V_T \ldots\ldots\ldots (3)$$

Comparing equation (2) and (3)

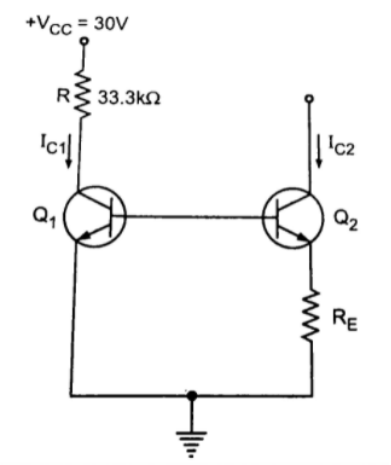
$$(I_{B2} + I_{C2})R_E = ln\left(\frac{I_{C1}}{I_{C2}}\right) \times V_T$$

Neglecting the value of I_{B2} $for\ large\ value\ of\ \beta$,

$$I_{C2} \times R_E = ln\left(\frac{I_{C1}}{I_{C2}}\right) \times V_T \ldots\ldots (4)$$

Problem 1

For the Widlar current source shown in the Fig, design the value of R_E to get I_{C2} as 20 μA. Assume V_{BE} = 0.7 V. Neglect base current.



Solution:

As the Base current is neglected,

$$I_{C1} = \frac{V_{CC} - V_{BE}}{R}$$

$$I_{C1} = \frac{30 - 0.7}{33.3 \times 10^3} = 0.8798\ mA$$

$$I_{C2} = 20\mu A$$

$$I_{C2} \times R_E = V_T \times ln\left(\frac{I_{C1}}{I_{C2}}\right)$$

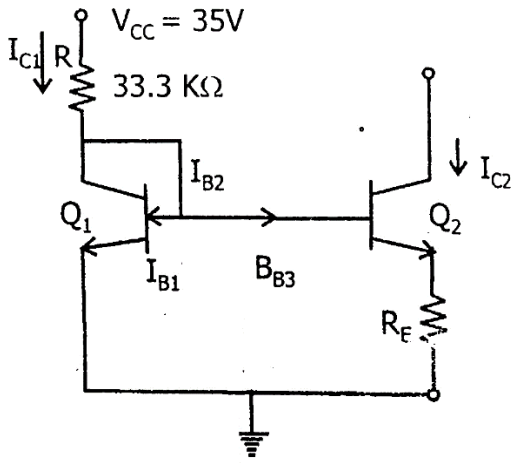
Assuming VT=26mV at room temperature

$$20 \times 10^{-6} \times R_E = 26 \times 10^{-3} \times ln\left(\frac{0.8798\ mA}{20\mu A}\right)$$

$$R_E = 4.92\Omega$$

Problem 2

For the widlar current source shown in Fig design the value R_E to get Ic as 25 mA. Assume V_{BE} = 0.7 V neglect base current.



$$I_{C1} = \frac{V_{CC} - V_{BE}}{R}$$

$$I_{C1} = \frac{35 - 0.7}{33.3K\Omega} = 1.03mA$$

$$I_{C2} = 25mA$$

$$I_{C2} \times R_E = V_T \times ln\left(\frac{I_{C1}}{I_{C2}}\right)$$

Assuming VT=26mV at room temperature

$$25 \times 10^{-3} \times R_E = 26 \times 10^{-3} \times ln\left(\frac{1.03\ mA}{25\mu A}\right)$$

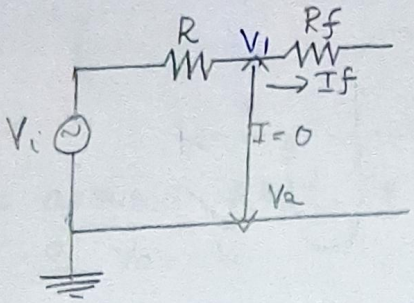
$$R_E = 3.867K\Omega$$

MODULE-2

APPLICATIONS OF OP-AMP

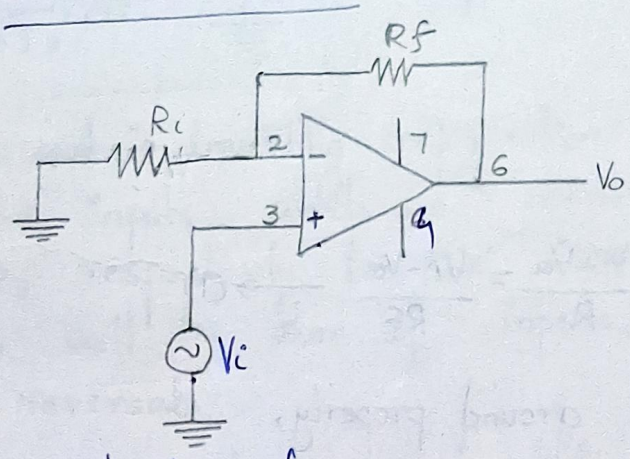
VIRTUAL GROUND PROPERTY

This means the differential input voltage between inverting and non-inverting terminals essentially zero.



From the figure there is a virtual shot between 2 input terminals, but no current flows from input terminals to this ground. The 2 input terminals of OP-AMP are always at same potential w.r.t ground.

NON-INVERTING AMPLIFIER (SCALE CHANGER)



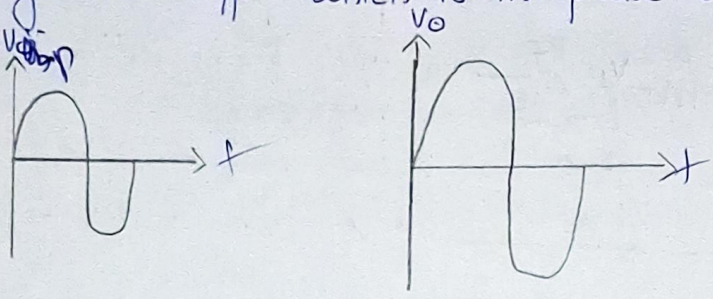
Voltage divider rule

$$Vi = Vo \times \frac{Ri}{Ri + Rf}$$

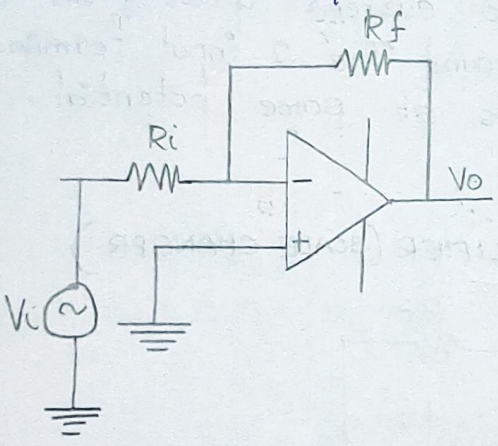
$$\frac{V_o}{V_i} = \frac{R_f + R_i}{R_i}$$

$$A_v = 1 + \frac{R_f}{R_i}$$, gain of non-inverting amplifier.

On non-inverting amplifier the input is applied to the non-inverting input terminal and we will get the o/p which is in phase with input.



INVERTING AMPLIFIER / SIGN CHANGER



From figure $\frac{V_i - V_a}{R_i} = \frac{V_A - V_o}{R_f}$ ⟶ (1)

Due to virtual ground property,

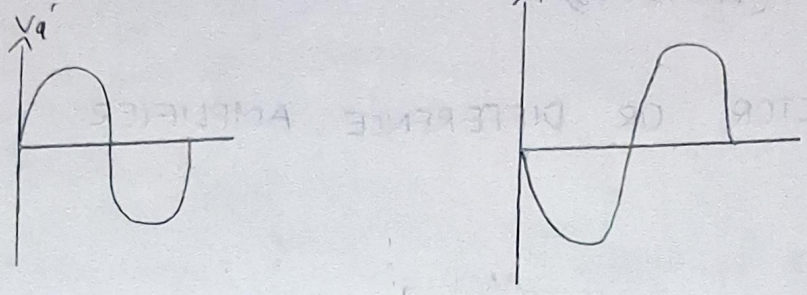
$V_i = 0$

Eqn (1) becomes

$$\frac{V_i}{R_i} = \frac{-V_o}{R_f}$$

$\frac{Vo}{Vi} = \frac{-Rf}{Ri} = Av$, gain of inverting amplifier.

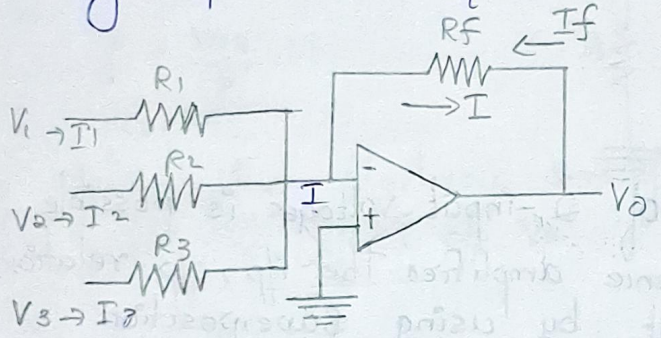
In the inverting amplifier, the input is given to inverting termind and so the o/p generated will be in out-of phase with i/p.



Let us assume $Rf = Ri$, $\forall$

So $Vo = -Vi$

Summing Amplifier or Adder Circuit



It is used in inverting configuration where V_1, V_2, V_3 are the inputs which are connected through R_1, R_2, R_3 respectively to the inverting terminal. The o/p will be sum of inputs, with the phase reversal.

From figure $I = I_1 + I_2 + I_3$

Since $I = -If$

$-If = I_1 + I_2 + I_3$

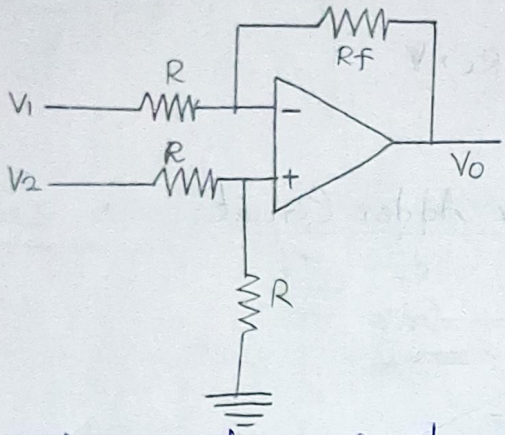
$$\frac{-V_o}{R_f} = \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}$$

If $R_1 = R_2 = R_3 = R_f = R$

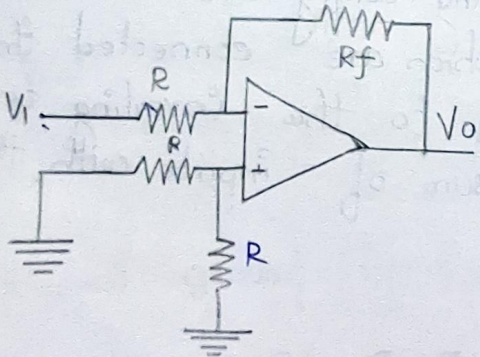
$$-V_o = V_1 + V_2 + V_3$$

$$V_o = -(V_1 + V_2 + V_3)$$

SUBSTRACTOR OR DIFFERENCE AMPLIFIER



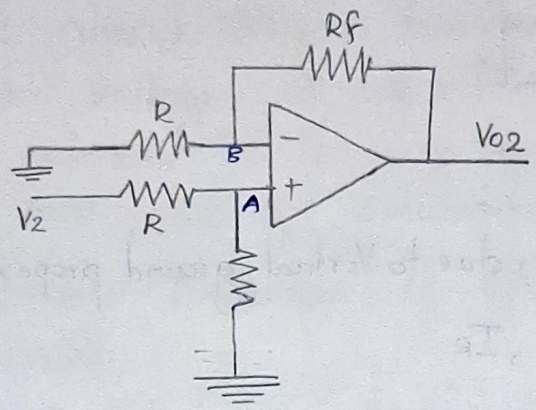
The substraction of 2-input voltages is possible with using difference amplifier. The i/p, o/p relation can be found out by using superposition theorem.



$$V_{o1} = -\frac{R_f}{R_i} \times V_1$$

If $R_f = R$

$V_{o1} = -V_1$



$V_A = V_2 + \frac{R}{2R}$

$V_B = V_A = \frac{V_2}{2} \rightarrow (1)$

V_A will couple to the -ve terminal of OP-AMP

so $V_B = V_A$

$\therefore V_B = V_{o2} \times \frac{R}{2R} = \frac{V_{o2}}{2} \rightarrow (2)$

Equate eqn (1) and eqn (2)

$$\frac{V_2}{2} = \frac{V_{o2}}{2}$$

$$V_2 = V_{o2}$$

By taking the algebraic sum of V_{o1} and V_{o2} we can have the final o/p V_o

$$V_o = V_{o1} + V_{o2}$$

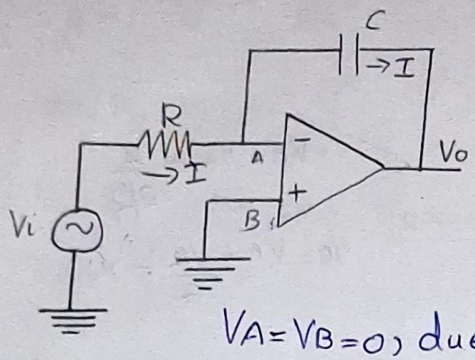
$$= -V_1 + V_2$$

$$V_o = V_2 - V_1$$

INTEGRATOR

Integrator is a circuit whose o/p voltage is the integral of i/p voltage. An integrator without OP-AMP or transistor, is called passive Integrator.

While an integrator with OP-AMP active integrator



$V_A = V_B = 0$, due to Virtual ground property

Current through resistor, I_R

$$I_R = \frac{(V_i - V_A)}{R} = \frac{V_i}{R} \longrightarrow (1)$$

Current through capacitor

$$I_C = C \cdot \frac{dv}{dt} = C\frac{(V_A - V_o)}{dt}$$

$$I_C = C\frac{V_o}{dt}$$

$$I_C = -C\frac{dV_o}{dt} \longrightarrow (2)$$

Since current through resistor = Current through capacitor

$$I_R = I_C$$

$$= \frac{V_i}{R} = -C\frac{dV_o}{dt}$$

Integrate both sides,

$$= \frac{1}{R}\int V_i - C\int \frac{dV_o}{dt}$$

$$= \frac{1}{R}\int V_i = -CV_o$$

So $$V_o = \frac{-1}{RC}\int V_i dt$$

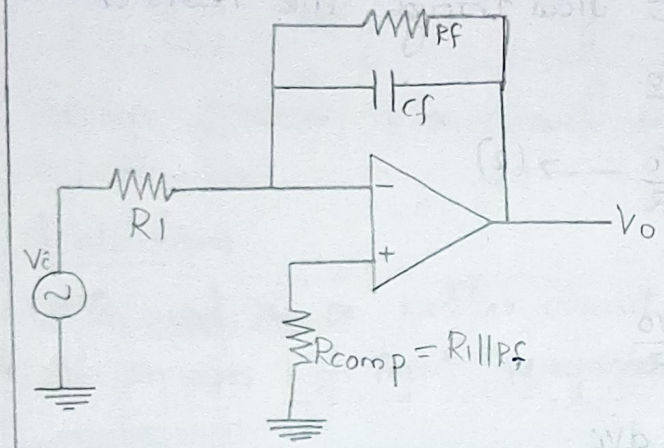
LIMITATIONS OF IDEAL INTEGRATOR

The OP-AMP has input offset voltage and input bias current. These two parameters produce an error voltage at output. This may cause OP-AMP to saturate. It is very difficult to pull the OP-AMP out of saturation.

Another limitation of ideal OP-AMP integrator is its low bandwidth.

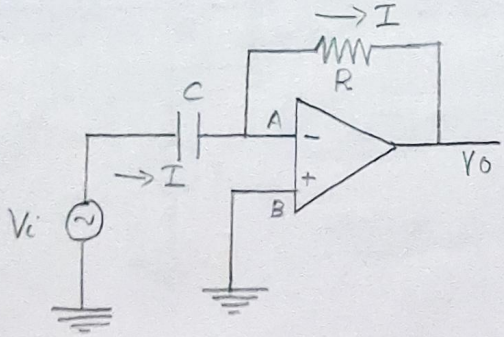
Infinite gain at low frequencies, At DC c acts as a open circuit

PRACTICAL INTEGRATOR Noise



Here the resistance Rcomp or Compensation resistor is used to overcome errors due to offset voltage and bias current and Rf reduces the voltage gain at low frequency and there by preventing the OP-AMP from saturation.

DIFFERENTIATOR



In this circuit the o/p is proportional to differential of input voltage. Here the terminal B is connected to ground and so the potential at B is will be coupled to terminal A

$\therefore V_A = V_B = 0$

Now the current through the capacitor,

$$I = C \frac{d}{dt}[V_i - V_A] \quad (V_A = 0)$$

$$I = C \frac{dV_i}{dt} \longrightarrow (1)$$

The same current I flow through the resistor

$$I = \frac{V_A - V_o}{R}$$

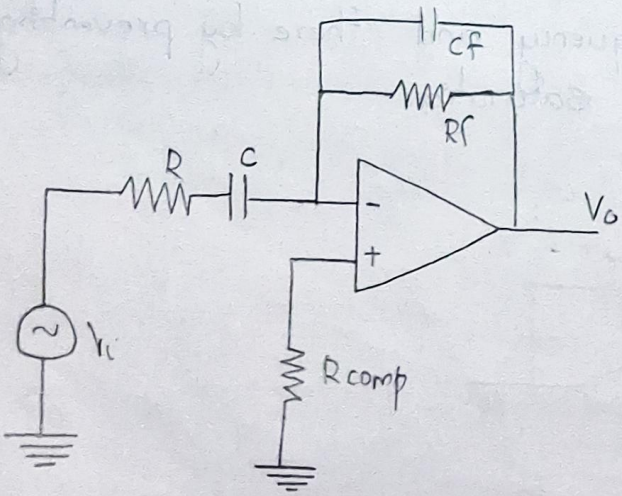
$$I = \frac{-V_o}{R} \longrightarrow (2)$$

Equate eqn(1) and eqn(2)

$$C\frac{dV_i}{dt} = -\frac{V_o}{R}$$

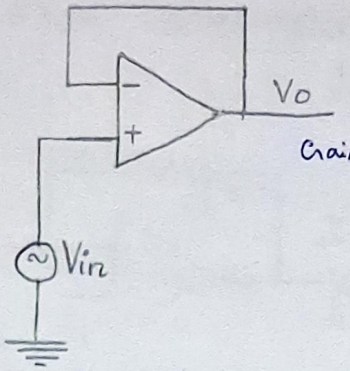
$$V_o = -RC\frac{dV_i}{dt}$$

PRACTICAL DIFFERENTIATOR.



Through this circuit we can acheive, bias compensation, noise reduction and gain stability

VOLTAGE FOLLOWER



Gain=1, Vo=Vin.

Voltage follower is a circuit whose gain is equal to 1 ie; $V_o = V_{in}$.

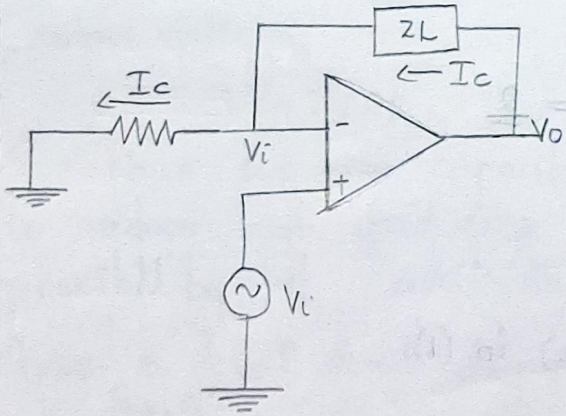
Applications

* It is used as a buffer circuit
* It provides high input impedance for the amplifier.

VOLTAGE TO CURRENT AND CURRENT TO VOLTAGE CONVERTERS

V TO I CONVERTER

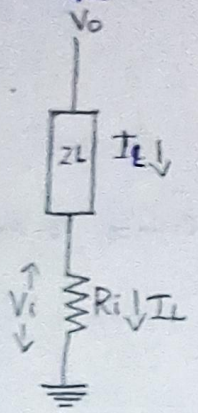
V to I converter with floated load



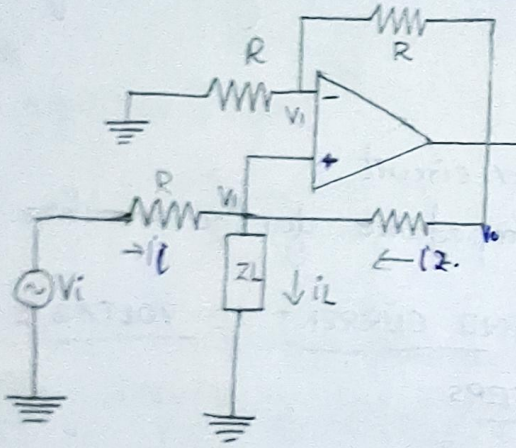
$$I_L = \frac{V_i}{R_i}$$

With floating load voltage to current converter the expression for load current, is

$$I_L = \frac{V_i}{R_i}$$



VTO I converter using grounded load.



$$i_L = i_1 + i_2.$$

$$i_L = \frac{V_i - V_1}{R} + \frac{V_o - V_1}{R}$$

$$i_L = \frac{V_i + V_o - 2V_i}{R} \rightarrow (1)$$

As it is configured in non-inverting type, the gain is equal to

$$\text{Gain} = 1 + \frac{Rf}{Ri} = 1 + \frac{R}{R} = 2$$

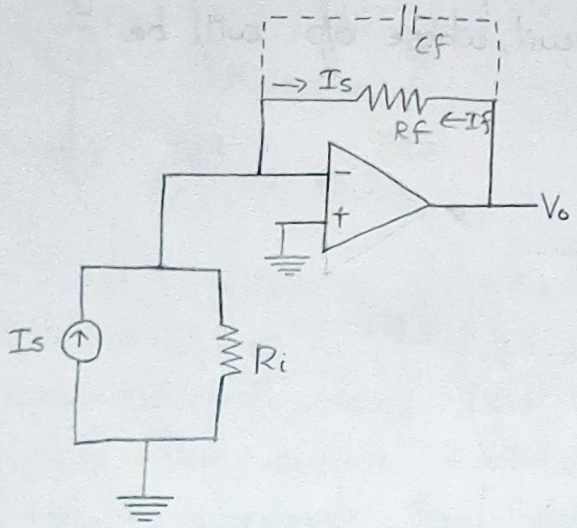
$$V_o = 2V_1 \rightarrow (2)$$

Then Substitute eqn (2) in (1)

$$i_L = \frac{V_i + 2V_i - 2V_i}{R}$$

$$\boxed{i_L = \frac{V_i}{R}}$$

CURRENT VOLTAGE CONVERTER



$$V_o = I_f R_f$$

Photovoltaic cell, photodiode etc gives an output current, which is directly proportional to incident energy or light. The current through the device can be converted into voltage by using current to voltage converter.

On figure, the entire source current Is flows through feedback resistance Rs and expression for output voltage,

$$V_f = I_f R_f$$

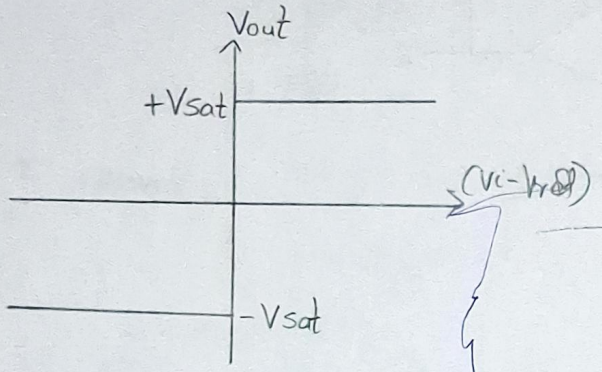
Sometimes we use capacitor cf in the feedback to reduce high frequency noise and the possibility of oscillations.

(2) Explain in detail about logarithmic and antilog amplifiers. Fig, Eqn.

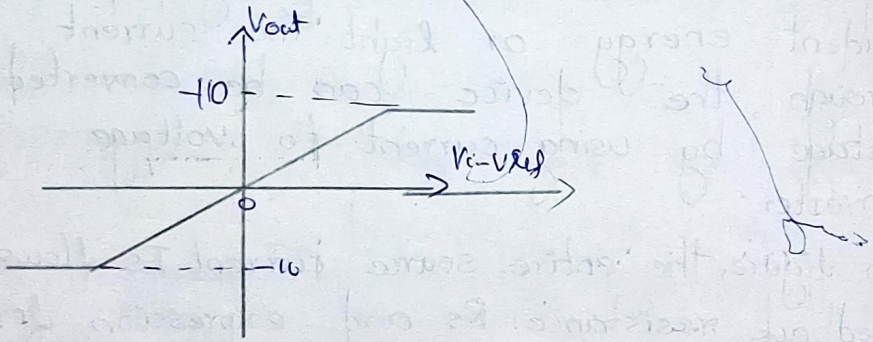
COMPARATORS

Comparator

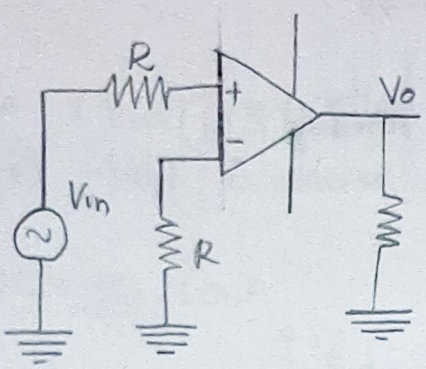
A comparator is a circuit which a signal voltage applied at one of the input with a non-reference voltage at the other input. It is basically an open-loop OP-AMP circuit, whose o/p will be ± or - Vsat.

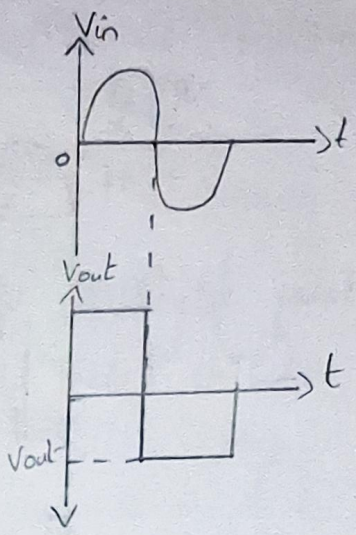


PRACTICAL CHARACTERISTICKS



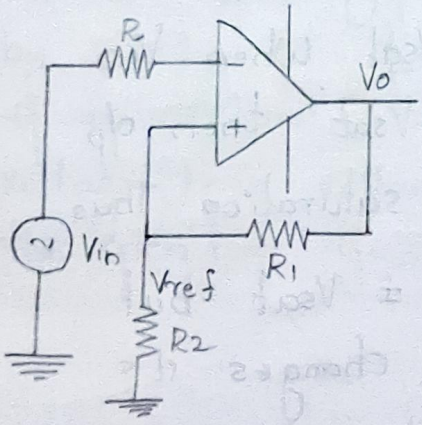
ZERO CROSSING DETECTOR

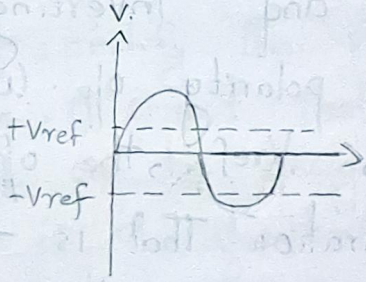




In a zero crossing detector, the reference voltage is set to zero. Figure shows a non-inverting zero crossing detector, where input is given to non-inverting terminal. The output switches between +Vsat and -Vsat whenever the input signal crosses the zero value. It is a sine wave to square wave convertor.

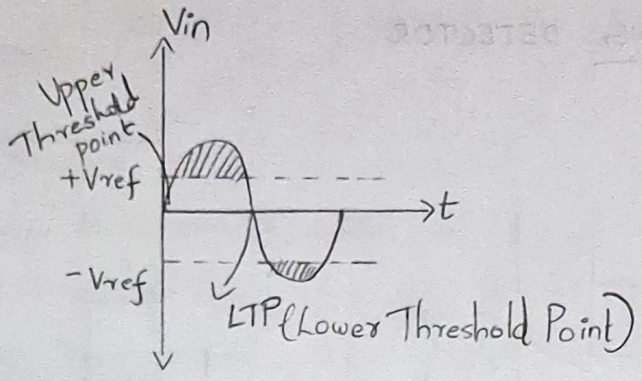
SCHMITT TRIGGER

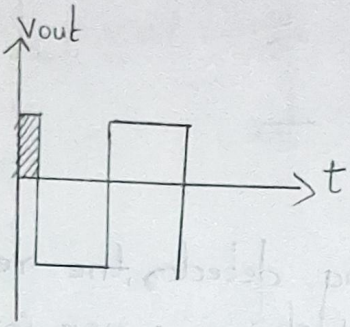




$$V_{ref} = +V_{sat} \times \frac{R_2}{R_1+R_2}$$

$$V_{ref} = -V_{sat} \times \frac{R_2}{R_1+R_2}$$





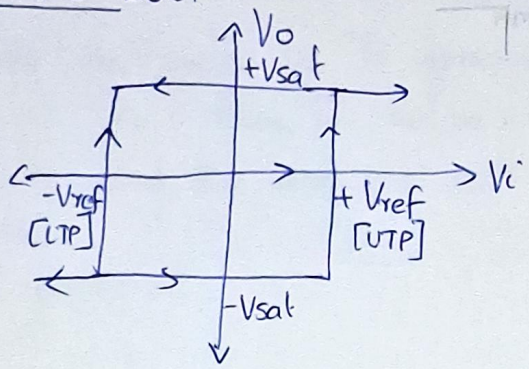
Schmitt Trigger is a sine to square wave converter which uses a -ve feedback. Here the i/p applied to the inverting terminal and inverting mode produced opposite polarity o/p. When Vin is slightly more +ve than Vref, the o/p gets drives into -ve saturation. That is -Vsat. When Vin becomes more -ve than -Vsat then o/p gets driven into +ve saturation. Thus o/p voltage is always ± Vsat but voltage at which it changes its state can be controlled with R1 and R2 which forms voltage divider

$$+V_{ref} = +V_{sat} \times \frac{R_2}{R_1+R_2}$$

$$-V_{ref} = -V_{sat} \times \frac{R_2}{R_1+R_2}$$

Here $+V_{ref}$ is called upper threshold point (UTP) $-V_{ref}$ is lower threshold point (LTP)

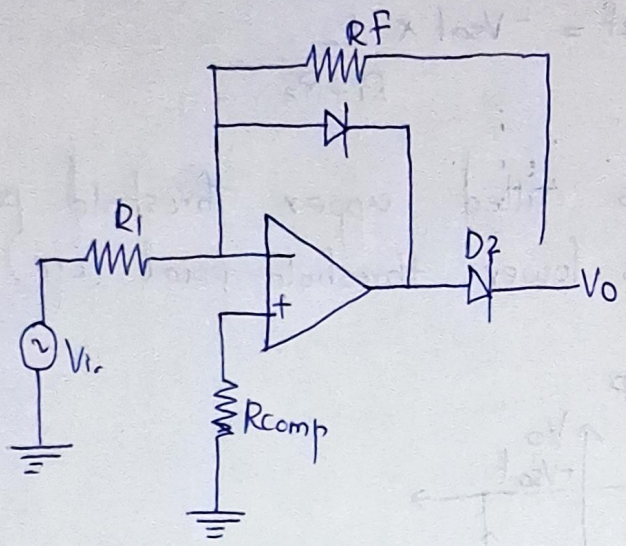
HYSTERISIS LOOP



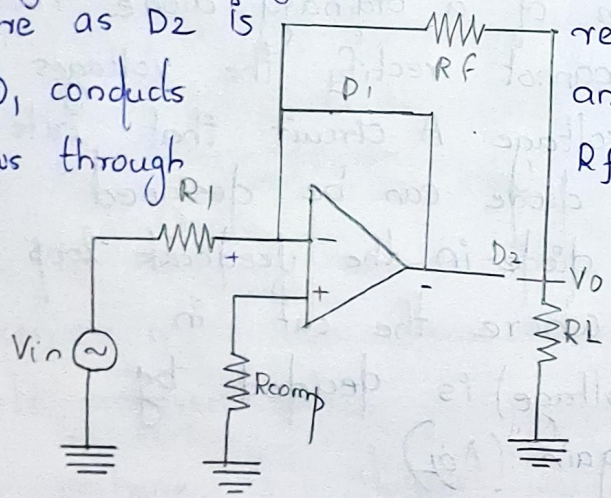
PRECISION RECTIFIER

The major function of a ordinary diode rectifier is that it cannot rectify the voltages below knee voltage. A circuit that acts as a ideal diode can be designed by placing a diode in the feedback loop of a OP-AMP where the cut in voltage (knee voltage) is decided by the open loop gain (A_{OL})

PRECISION HALFWAVE RECTIFIER

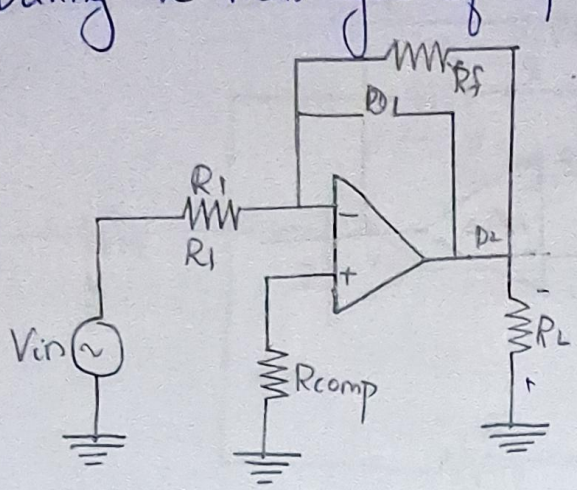


During +ve half cycle diode D_1 become forward biased where as D_2 is reverse biased.
∴ D_1 conducts and practically no current flows through Rf=0

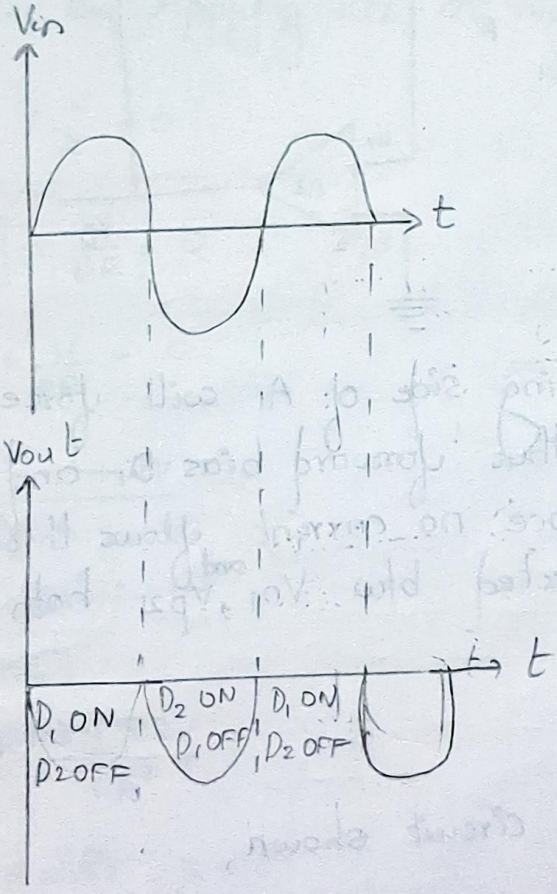


So the o/p voltage Vo=0

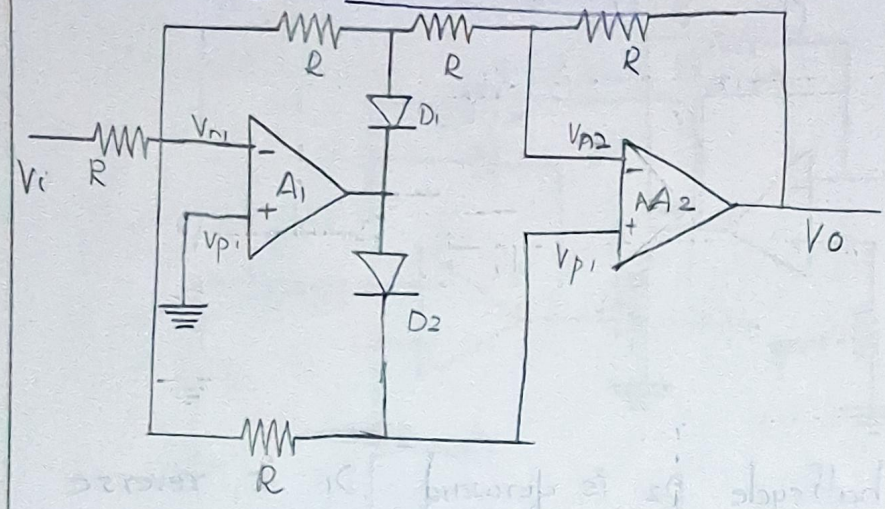
During -ve half cycle of input



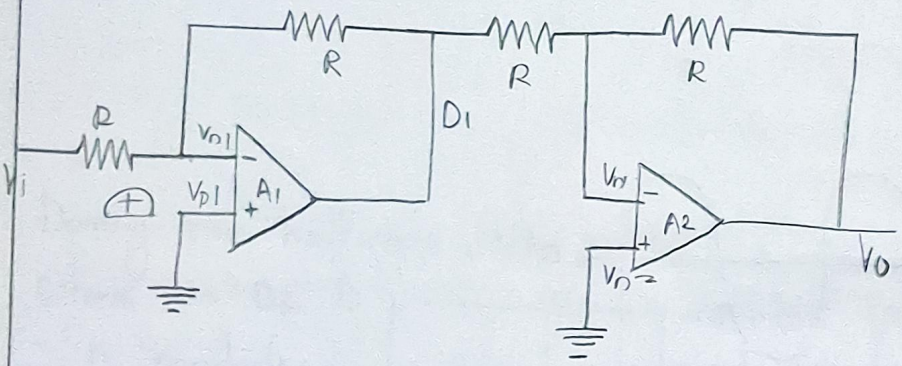
During -ve halfcycle D_2 is forward D_1 is reverse biased at this time, the entire current flows through R_L and R_f and we will get an o/p voltage across R_L.



PRECISION FULLWAVE RECTIFIER



During +ve halfcycle, Vin > 0



When Vin>0, the inverting side of A_1 will force the o/p to swing -ve, thus forward bias D_1 and reverse bias D_2. Since no current flows through resistance R connected b/w V_{n1} and V_{p2} both are at equipotential ie;

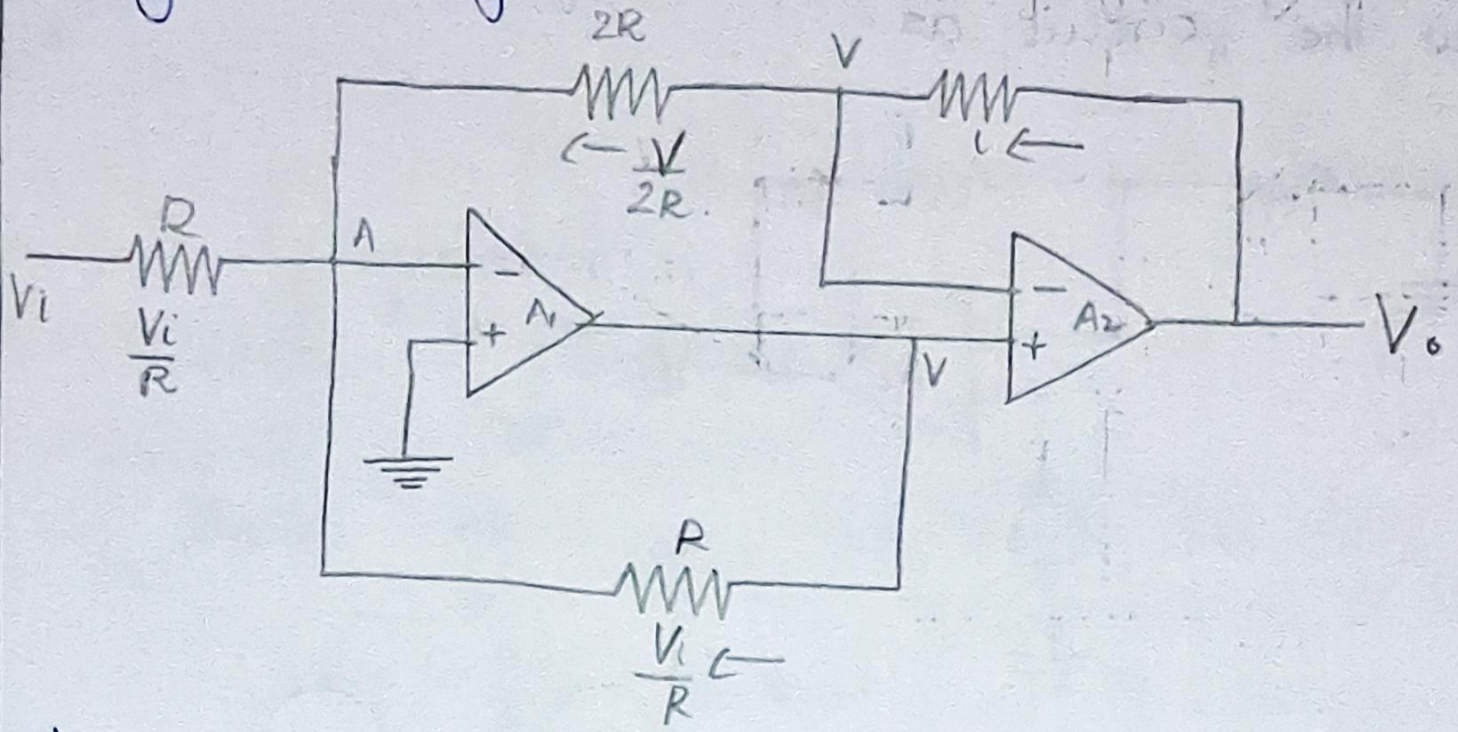
ie; $V_{n1} = V_{p2} = 0$

From the equivalent circuit shown,

$$V_o = V_{in}\left(\frac{-R}{R}\right) \times \left(\frac{-R}{R}\right)$$

$$V_o = V_{in}$$

During -ve half cycle



During -ve half cycle the op of A_1 swings to +ve making D_1 reverse biased and D_2 forward biased. So By Applying KCL at Node A

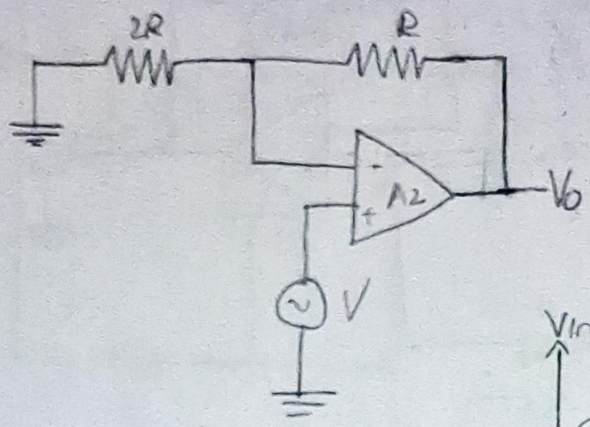
$$\frac{V_i}{R} + \frac{V}{2R} + \frac{V}{R} = 0$$

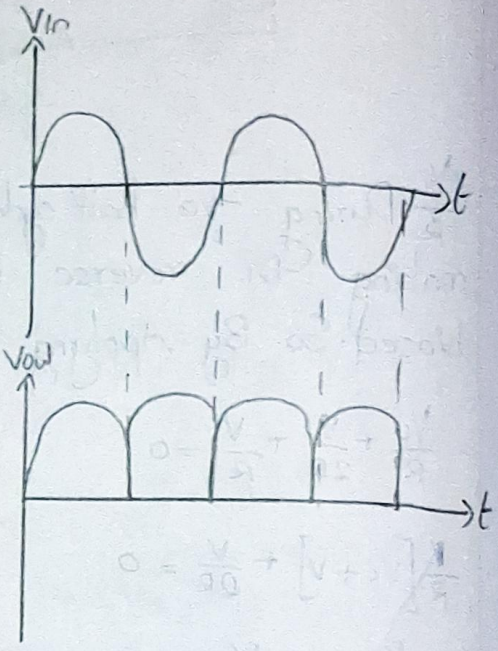
$$= \frac{V_i}{R} + \frac{RV + 2RV}{2R^2}$$

$$\frac{V_i}{R} + \frac{3RV}{3R^2} = 0$$

$$V = \frac{-2V_i}{3}$$

In order to get final o/p in terms of V we will redraw the circuit as.





$$V_o = V\left[1 + \frac{R}{2R}\right]$$

$$= V\left[\frac{2R+R}{2R}\right]$$

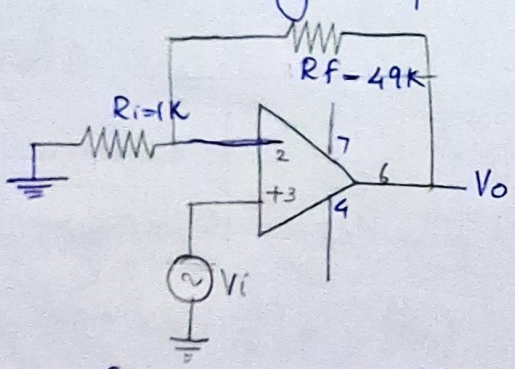
$$= V\left[\frac{3R}{2R}\right]$$

$$V_o = V \times 3/2$$

$$V_o = -\frac{2V_i}{3} \times \frac{3}{2}$$

$$\underline{V_o = -V_i}$$

2 Design a non-inverting amplifier for a gain = 50



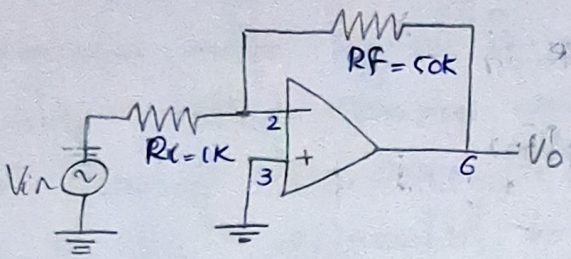
$R_i = 1K$

$$\text{Gain} = \frac{1+Rf}{Ri} \qquad 50 = \frac{1}{1} + \frac{Rf}{Ri}$$

$$50 = \frac{Ri + Rf}{Ri} \qquad 50 = 1 + Rf$$

$$50 - 1 = Rf, \quad \underline{Rf = 49R}$$

7. Design an inverting Amplifier for gain = 50



$$\text{Gain} = \frac{-RF}{Ri}$$

$$50 = \frac{-RF}{1} \qquad RF = 50K$$

$$V_{LT} = \frac{100}{50100} \times (-14) = -28 \text{ mV}$$

Example 5.3

A Schmitt trigger with the upper threshold level $V_{UT} = 0$ V and hysteresis width $V_H = 0.2$ V converts a 1 kHz sine wave of amplitude $4V_{pp}$ into a square wave. Calculate the time duration of the negative and positive portion of the output waveform.

Solution

$$V_{UT} = 0$$

$$V_H = V_{UT} - V_{LT} = 0.2 \text{ V}$$

So, $V_{LT} = -0.2$ V

In Fig. 5.9, the angle θ can be calculated as

$$-0.2 = V_m \sin(\pi + \theta) = -V_m \sin\theta = -2 \sin\theta$$

$$\theta = \text{arc sin } 0.1 = 0.1 \text{ radian}$$

The period, $T = 1/f = 1/1000 = 1$ ms

$$\omega T_\theta = 2\pi\ (1000)\ T_\theta = 0.1$$

$$T_\theta = (0.1/2\pi) \text{ ms} = 0.016 \text{ ms}$$

So, $T_1 = T/2 + T_\theta = 0.516$ ms

and $T_2 = T/2 - T_\theta = 0.484$ ms

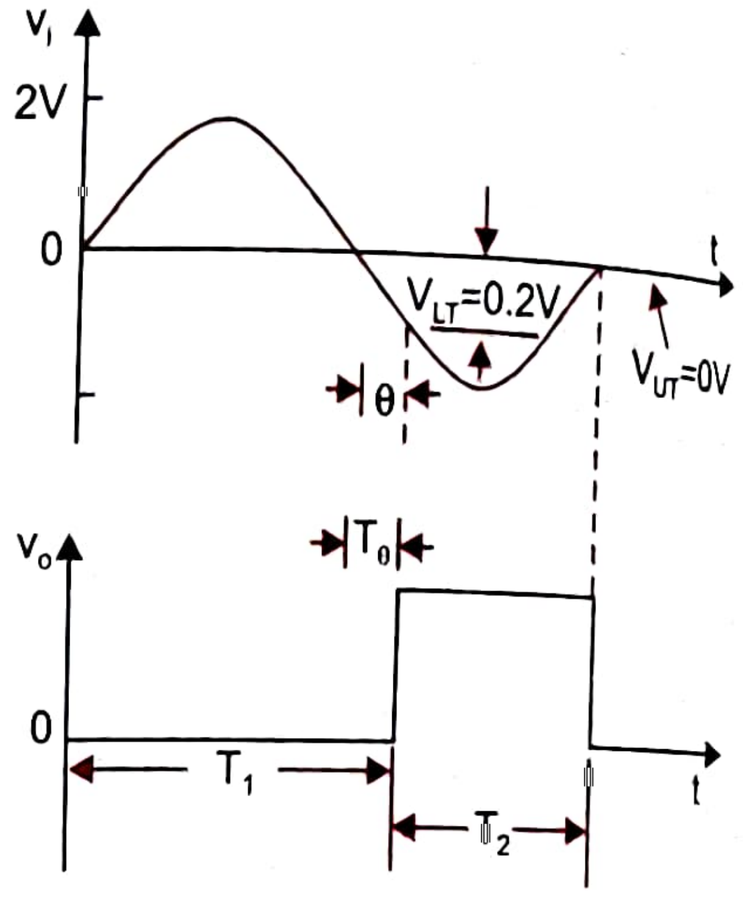


Fig. 5.9 Circuit for Example 5.3

5.4 SQUARE WAVE GENERATOR (ASTABLE MULTIVIBRATOR)

A simple op-amp square wave generator is shown in Fig. 5.10 (a). Also called a ***free running oscillator,*** the principle of generation of square wave output is to force an op-amp to operate in the saturation region. In Fig. 5.10 (a) fraction $\beta = R_2/(R_1 + R_2)$ of the output is fed back to the (+) input terminal. Thus the reference voltage V_{ref} is βv_o and may take values as

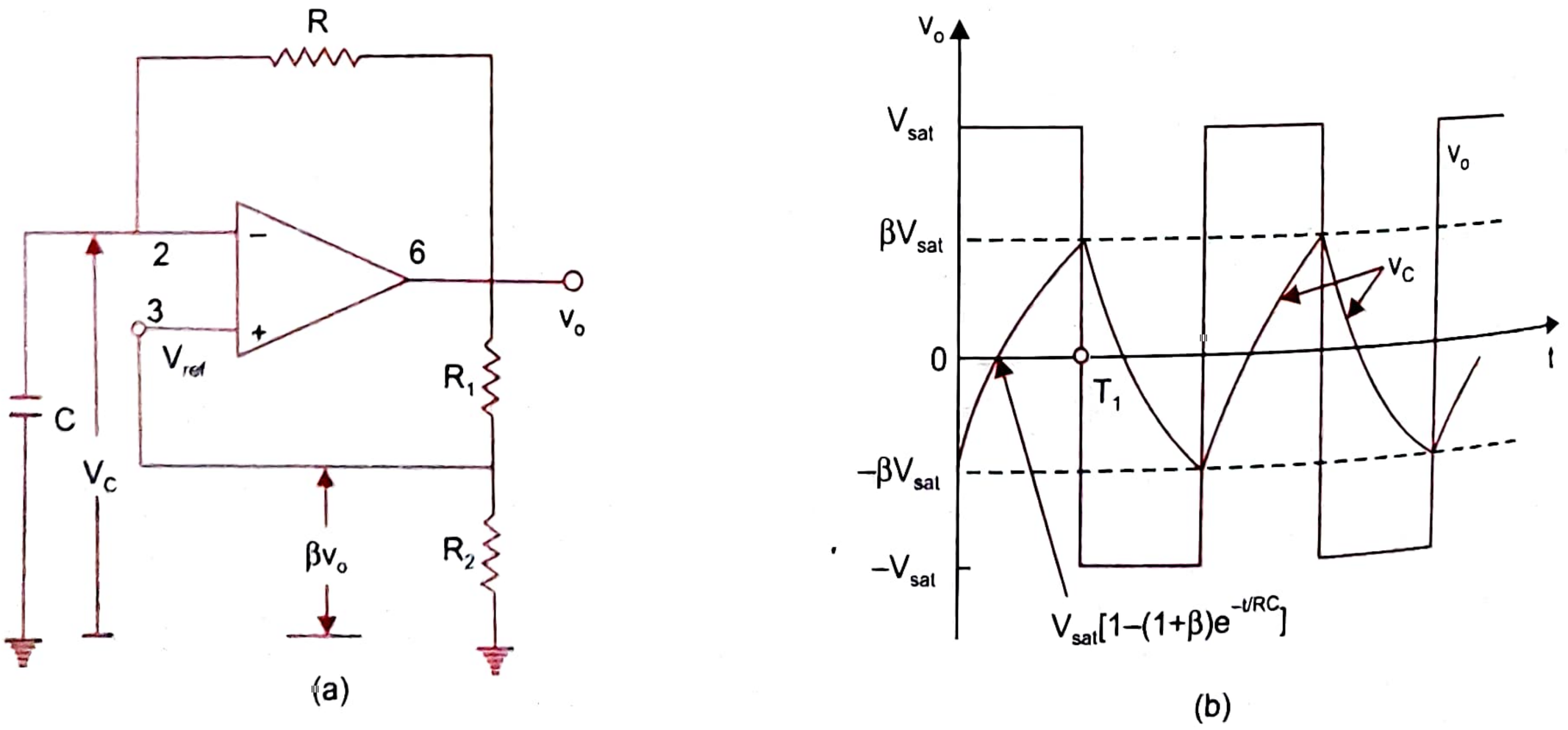


Fig. 5.10 (a) Simple op-amp square wave generator (b) Waveforms

$+\beta V_{sat}$ or $-\beta V_{sat}$. The output is also fed back to the (–) input terminal after integrating by means of a low-pass RC combination. Whenever input at the (–) input terminal just exceeds V_{ref} switching takes place resulting in a square wave output. In astable multivibrator, both the states are quasi stable.

Consider an instant of time when the output is at $+V_{sat}$. The capacitor now starts charging towards $+V_{sat}$ through resistance R, as shown in Fig. 5.10 (b). The voltage at the (+) input terminal is held at $+\beta V_{sat}$ by R_1 and R_2 combination. This condition continues as the charge on C rises, until it has just exceeded $+\beta V_{sat}$, the reference voltage. When the voltage at the (–) input terminal becomes just greater than this reference voltage, the output is driven to $-V_{sat}$. At this instant, the voltage on the capacitor is $+\beta V_{sat}$. It begins to discharge through R. that is, charges toward $-V_{sat}$. When the output voltage switches to $-V_{sat}$, the capacitor charges more and more negatively until its voltage just exceeds $-\beta V_{sat}$. The output switches back to $+V_{sat}$. The cycle repeats itself as shown in Fig. 5.10 (b).

The frequency is determined by the time it takes the capacitor to charge from $-\beta V_{sat}$ to $+\beta V_{sat}$ and vice versa. The voltage across the capacitor as a function of time is given by,

$$v_c(t) = V_f + (V_i - V_f)e^{-t/RC} \tag{5.4}$$

where, the final value, $V_f = +V_{sat}$

and the initial value, $V_i = -\beta V_{sat}$

Therefore,

$$v_c(t) = V_{sat} + (-\beta V_{sat} - V_{sat})\, e^{-t/RC}$$

or

$$v_c(t) = V_{sat} - V_{sat}\,(1 + \beta)\, e^{-t/RC} \tag{5.5}$$

At $t = T_1$, voltage across the capacitor reaches βV_{sat} and switching takes place. Therefore,

$$v_c(T_1) = \beta V_{sat} = V_{sat} - V_{sat}\,(1+\beta)e^{-T_1/RC} \tag{5.6}$$

After algebraic manipulation, we get,

$$T_1 = RC \ln \frac{1+\beta}{1-\beta} \tag{5.7}$$

This give only one half of the period.

Total time period

$$T = 2T_1 = 2RC \ln \frac{1+\beta}{1-\beta} \tag{5.8}$$

and the output wave form is symmetrical.

If $R_1 = R_2$, then $\beta = 0.5$, and $T = 2RC \ln 3$. And for $R_1 = 1.16R_2$, it can be seen that $T = 2\,RC$

or

$$f_0 = \frac{1}{2RC}$$

The output swings from $+V_{sat}$ to $-V_{sat}$, so,

$$v_o \text{ peak-to-peak} = 2\ V_{sat} \tag{5.9}$$

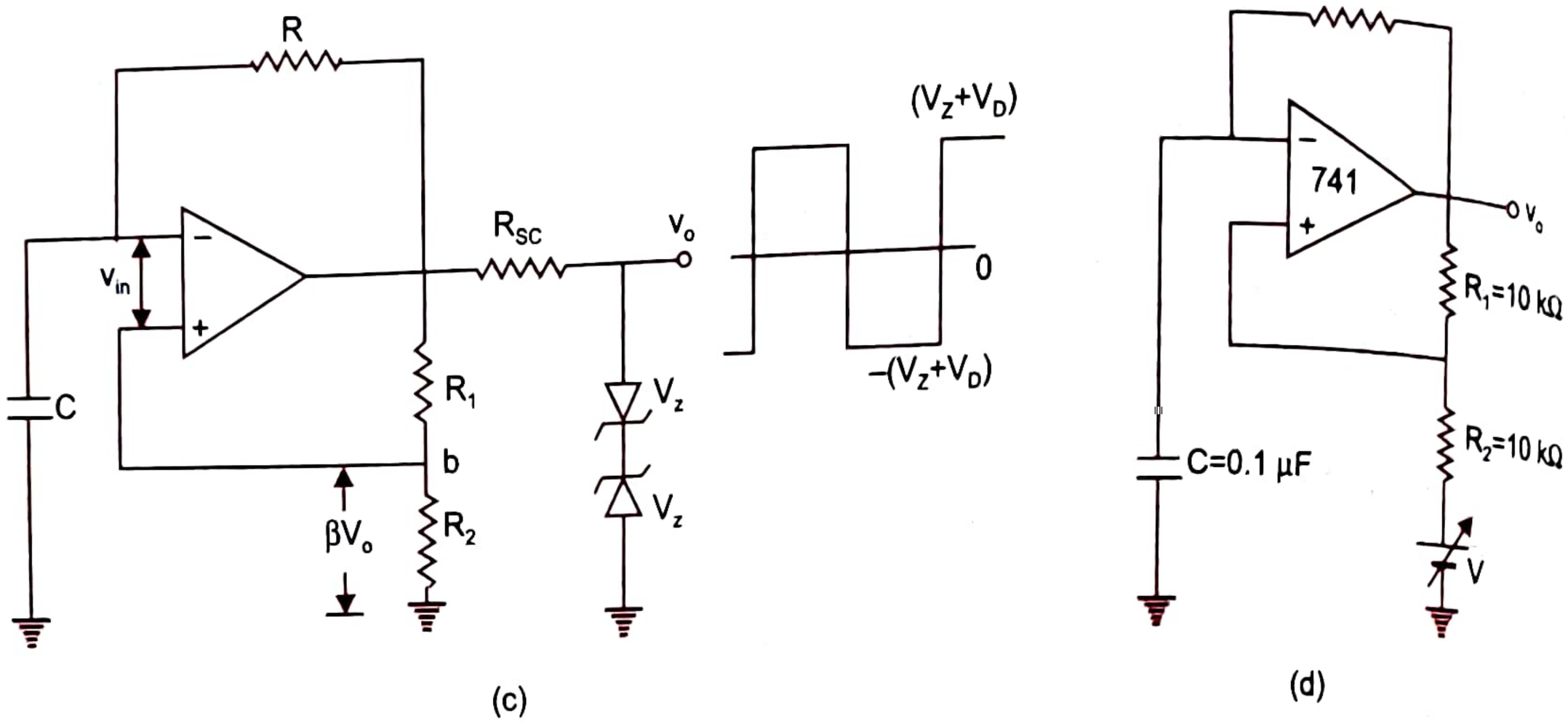


Fig. 5.10 (c) Use of back to back zener diodes. (d) Asymmetric square wave generator

The peak to peak output amplitude can be varied by varying the power supply voltage. However, a better technique is to use back to back zener diodes as shown in Fig. 5.10 (c). The output voltage is regulated to $\pm (V_Z + V_D)$ by the zener diodes.

$$v_o \text{ peak-to-peak} = 2 (V_Z + V_D) \tag{5.10}$$

Resistor R_{sc} limits the currents drawn from the op-amp to,

$$I_{sc} = \frac{V_{sat} - V_Z}{R_{sc}} \tag{5.11}$$

This circuit works reasonably well at audio frequencies. At higher frequencies, however, slew-rate of the op-amp limits the slope of the output square wave.

If an ***asymmetric square wave*** is desired, then zener diodes with different break down voltages V_{Z1} and V_{Z2} may be used. Then the output is either V_{o1} or V_{o2}, where $V_{o1} = V_{Z1} + V_D$ and $V_{o2} = V_{Z2} + V_D$. It can be easily shown that the positive section is given by,

$$T_1 = RC \ln \frac{1+\beta V_{o2}/V_{o1}}{1-\beta} \tag{5.12}$$

The duration of negative section T_2 will be the same as given by Eq. (5.12) with V_{o1} and V_{o2} interchanged.

An alternative method to get asymmetric square wave output is to add a dc voltage source V in series R_2 as shown in Fig. 5.10 (d). Now the capacitor C swings between the voltage levels $(\beta V_{sat} + V)$ and $(-\beta V_{sat} + V)$. If the voltage source V is made variable, voltage to frequency conversion can be achieved though the variation will not be linear.

5.5 MONOSTABLE MULTIVIBRATOR

Monostable multivibrator has one stable state and the other is quasi stable state. The circuit is useful for generating single output pulse of adjustable time duration in response to a triggering signal. The width of the output pulse depends only on external components connected to the op-amp. The circuit shown in Fig. 5.11(a) is a modified form of the astable multivibrator.

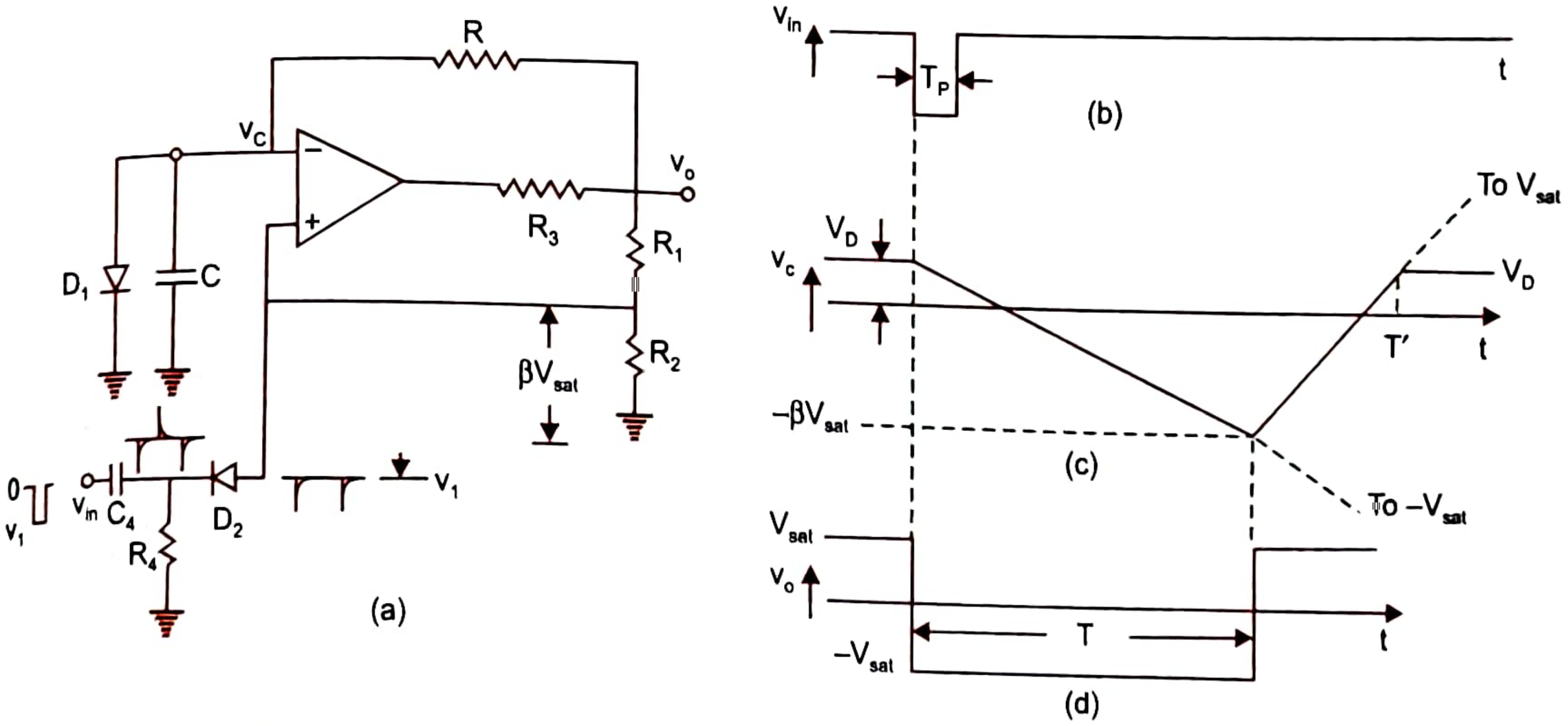


Fig. 5.11 (a) Monostable multivibrator, (b) Negative going triggering signal, (c) Capacitor waveform, (d) Output voltage waveform

A diode D_1 clamps the capacitor voltage to 0.7 V when the output is at $+V_{sat}$. A negative going pulse signal of magnitude V_1 passing through the differentiator R_4C_4 and diode D_2 produces a negative going triggering impulse and is applied to the (+) input terminal.

To analyse the circuit, let us assume that in the stable state, the output υ_o is at $+V_{sat}$. The diode D_1 conducts and υ_c the voltage across the capacitor C gets clamped to +0.7 V. The voltage at the (+) input terminal through R_1R_2 potentiometric divider is $+\beta V_{sat}$. Now, if a negative trigger of magnitude V_1 is applied to the (+) input terminal so that the effective signal at this terminal is less than 0.7 V, i.e. $([\beta V_{sat} + (-V_1)] < 0.7\text{ V})$, the output of the op-amp will switch from $+V_{sat}$ to $-V_{sat}$. The diode will now get reverse biased and the capacitor starts charging exponentially to $-V_{sat}$ through the resistance R. The voltage at the (+) input terminal is now $-\beta V_{sat}$. When the capacitor voltage υ_c becomes just slightly more negative than $-\beta V_{sat}$, the output of the op-amp switches back to $+V_{sat}$. The capacitor C now starts charging to $+V_{sat}$ through R until υ_c is 0.7V as capacitor C gets clamped to the voltage. Various waveforms are shown in Fig. 5.11 (b, c, d).

The pulse width T of monostable multivibrator is calculated as follows:

The general solution for a single time constant low pass RC circuit with V_i and V_f as initial and final values is,

$$\upsilon_o = V_f + (V_i - V_f)e^{-t/RC} \tag{5.13}$$

For the circuit, $V_f = -V_{sat}$ and $V_i = V_D$ (diode forward voltage).

The output υ_c is,

$$\upsilon_c = -V_{sat} + (V_D + V_{sat})\, e^{-t/RC} \tag{5.14}$$

at $t = T$,

$$\upsilon_c = -\beta V_{sat} \tag{5.15}$$

Therefore,

$$-\beta\, V_{sat} = -V_{sat} + (V_D + V_{sat})e^{-T/RC}$$

After simplification, pulse width T is obtained as

$$T = RC \ln \frac{(1 + V_D/V_{sat})}{1 - \beta} \tag{5.16}$$

where $\beta = R_2/(R_1 + R_2)$

If, $V_{sat} >> V_D$ and $R_1 = R_2$ so that $\beta = 0.5$, then

$$T = 0.69\ RC \tag{5.17}$$

For monostable operation, the trigger pulse width T_p should be much less than T, the pulse width of the monostable multivibrator. The diode D_2 is used to avoid malfunctioning by blocking the positive noise spikes that may be present at the differentiated trigger input.

It may be noted from Fig. 5.11 (b) that capacitor voltage v_c reaches its quiescent value V_D at $T' > T$. Therefore, it is essential that a recovery time $T' - T$ be allowed to elapse before the next triggering signal is applied. The circuit of Fig. 5.11 (a) can be modified to achieve voltage to time delay conversion as in the case of square wave generator. The monostable multivibrator circuit is also referred to as time delay circuit as it generates a fast transition at a predetermined time T after the application of input trigger. It is also called a gating circuit as it generates a rectangular waveform at a definite time and thus could be used to gate parts of a system.

5.6 TRIANGULAR WAVE GENERATOR

A triangular wave can be simply obtained by integrating a square wave as shown in Fig. 5.12 (a). It is obvious that the frequency of the square wave and triangular wave is the same as shown in Fig. 5.12 (b). Although the amplitude of the square wave is constant at $\pm V_{sat}$, the amplitude of the triangular wave will decrease as the frequency increases. This is because the reactance of the capacitor C_2 in the feedback circuit decreases at high frequencies. A resistance R_4 is connected across C_2 to avoid the saturation problem at low frequencies as in the case of practical integrator.

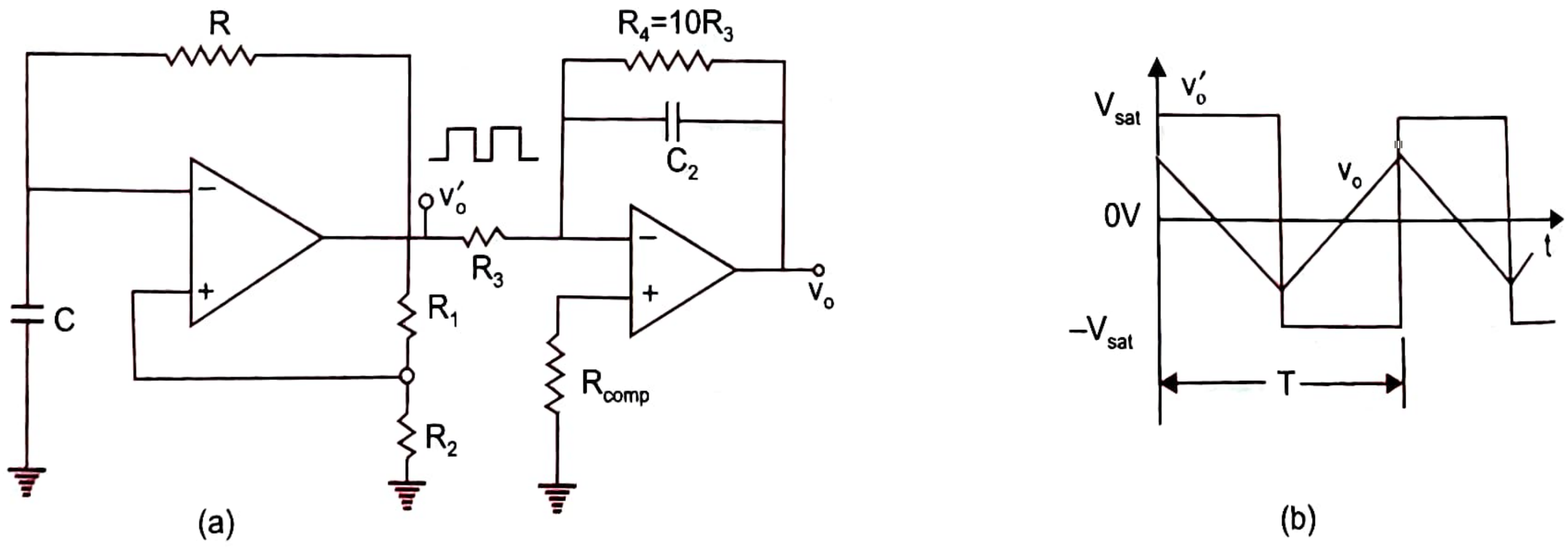
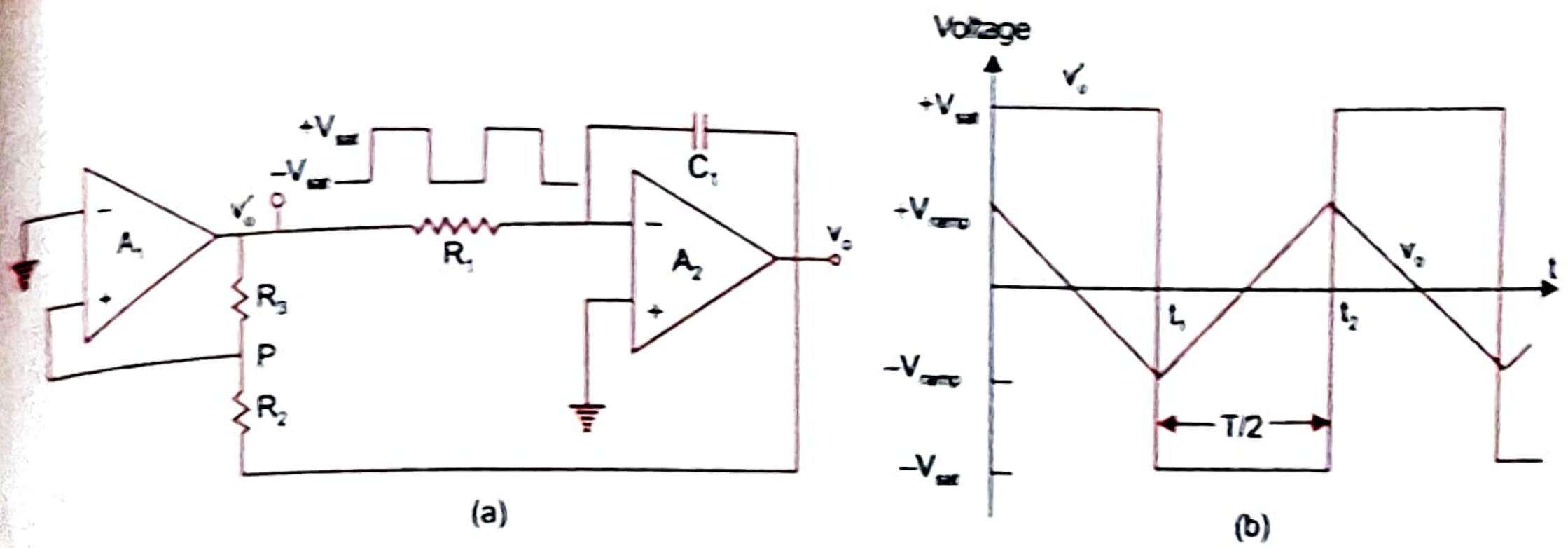


Fig. 5.12 (a) Triangular waveform generator, (b) Output waveform

Another triangular wave generator using lesser number of components is shown in Fig. 5.13 (a). It basically consists of a two level comparator followed by an integrator. The output of the comparator A_1 is a square wave of amplitude $\pm V_{sat}$ and is applied to the (–) input terminal of the integrator A_2 producing a triangular wave. This triangular wave is fed back as input to the comparator A_1 through a voltage divider R_2R_3.



(a) (b)

Fig. 5.13 (a) Triangular waveform generator using lesser components, (b) Waveforms

Initially, let us consider that the output of comparator A_1 is at $+V_{sat}$. The output of the integrator A_2 will be a negative going ramp as shown in Fig. 5.13 (b). Thus one end of the voltage divider R_2R_3 is at a voltage $+V_{sat}$ and the other at the negative going ramp of A_2. At a time $t = t_1$, when the negative going ramp attains a value of $-V_{ramp}$, the effective voltage at point P becomes slightly less than 0 V. This switches the output of A_1 from positive saturation to negative saturation level $-V_{sat}$. During the time when the output of A_1 is at $-V_{sat}$, the output of A_2 increases in the positive direction. And at the instant $t = t_2$, the voltage at point P becomes just above 0 V, thereby switching the output of A_1 from $-V_{sat}$ to $+V_{sat}$. The cycle repeats and generates a triangular waveform. It can be seen that the frequency of the square wave and triangular wave will be the same. However, the amplitude of the triangular wave depends upon the RC value of the integrator A_2 and the output voltage level of A_1. The output voltage of A_1 can be set to desired level by using appropriate zener diodes. The frequency of the triangular waveform can be calculated as follows:

The effective voltage at point P during the time when output of A_1 is at $+V_{sat}$ level is given by,

$$-V_{ramp} + \frac{R_2}{R_2 + R_3}\left[+V_{sat} - (-V_{ramp})\right] \tag{5.18}$$

At $t = t_1$, the voltage at point P becomes equal to zero. Therefore, from Eq. (5.18),

$$-V_{ramp} = -\frac{R_2}{R_3}(+V_{sat}) \tag{5.19}$$

Similarly, at $t = t_2$, when the output of A_1 switches from $-V_{sat}$ to $+V_{sat}$,

$$V_{ramp} = \frac{-R_2}{R_3}(-V_{sat}) = \frac{R_2}{R_3}(V_{sat}) \tag{5.20}$$

Therefore, peak to peak amplitude of the triangular wave is,

$$v_o\,(\text{pp}) = +\,V_{ramp} - (-V_{ramp}) = 2\,\frac{R_2}{R_3}V_{sat} \tag{5.21}$$

The output switches from $-V_{ramp}$ to $+V_{ramp}'$ in half the time period $T/2$. Putting the values in the basic integrator equation

$$v_o = -\frac{1}{RC}\int v_i\,dt$$

$$v_o(\text{pp}) = -\frac{1}{R_1C_1}\int_0^{T/2}(-V_{sat})dt = \frac{V_{sat}}{R_1C_1}\left(\frac{T}{2}\right)$$

or,
$$T = 2\,R_1C_1\frac{v_o\,(\text{pp})}{V_{sat}} \tag{5.22}$$

Putting the value of v_o (pp) from Eq. (5.21), we get

$$T = \frac{4R_1C_1R_2}{R_3}$$

Hence the frequency of oscillation f_o is,

$$f_o = \frac{1}{T} = \frac{R_3}{4R_1C_1R_2} \tag{5.23}$$

Therefore, the triangular wave oscillates between + 7V and – 7V.

Sawtooth Wave Generator

The difference between the triangular and sawtooth waveforms is that the rise time of a triangular wave is always equal to its fall time. That is, the same amount of time is taken by the triangular wave to swing from $-V_{ramp}$ to $+V_{ramp}$ as from $+V_{ramp}$ to $-V_{ramp}$. On the other hand, the sawtooth waveform has unequal rise and fall times. That is, it may rise many times faster than it falls negatively, or vice versa. The triangular wave generator is as shown in Fig 5.14.

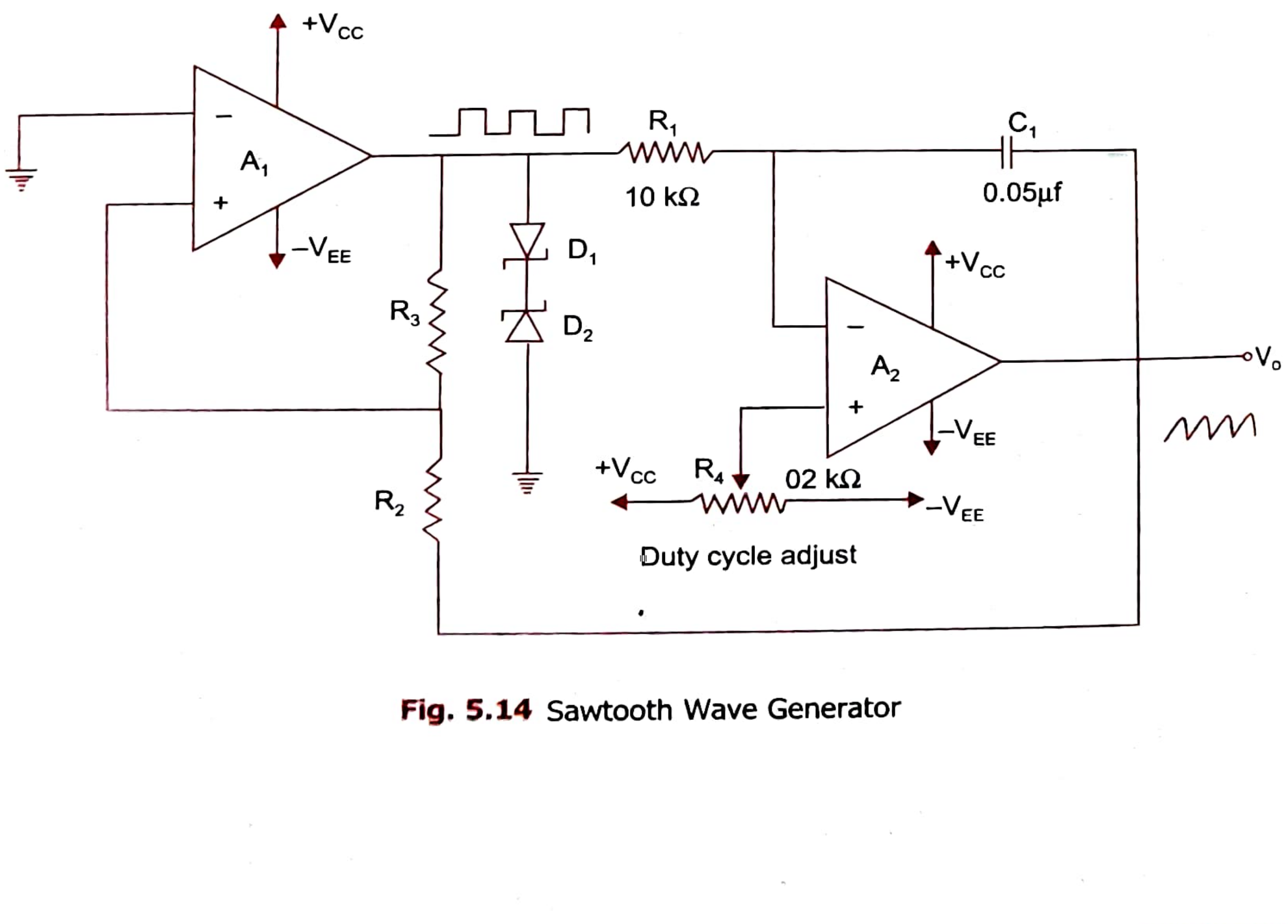


Fig. 5.14 Sawtooth Wave Generator

The triangular wave generator can be converted into a sawtooth wave generator by applying a variable dc voltage into the noninverting terminal of the integrator A_2. This can be accompalished by using the potentiometer and connecting it to the $+V_{CC}$ and $+V_{EE}$ as shown in Fig 5.14.

Depending on the R_4 setting, a certain dc level is inserted in the output of A_2. Now, suppose that the output of A_1 is a square wave and the potentiometer R_4 is adjusted for a certain dc level. This means that the output of A_2 will be a triangular wave, rising on some dc level that is a function of the R_4 setting. The duty cycle of the square wave will be determined by the polarity and amplitude of this dc level. A duty cycle less than 50% will then cause the output of A_2 to be a sawtooth. With the wiper at the center of R_4, the output of A_2 is a triangular wave. For any other position of R_4 wiper, the output is a sawtooth waveform. Specifically as the R_4 wiper is moved toward $-V_{EE}$, the rise time of the sawtooth wave becomes longer than the fall time as shown in Fig 5.15.

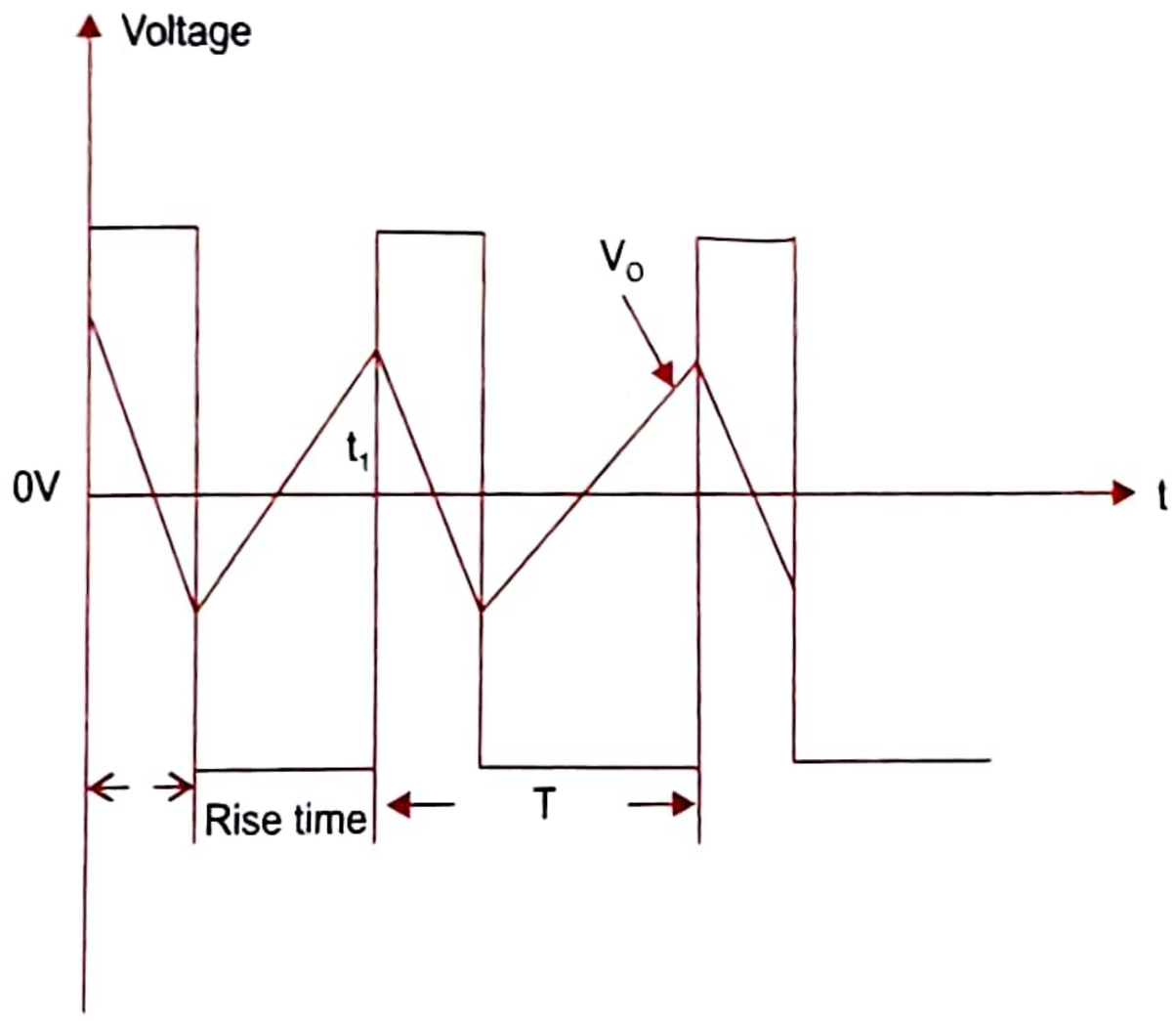


Fig. 5.15 Sawtooth waveform

On the otherhand, as the wiper is moved towards $+V_{CC}$, the fall time becomes longer than the rise time. Also, the frequency of the Sawtooth decreases as R_4 is adjusted towards $+V_{CC}$ or $-V_{EE}$

However, the amplitude of the sawtooth wave is independent of the R_4 setting.

Example 5.4

Design a sawtooth wave generator for 10V peak and frequency of 200 Hz. Assume $V_i = 2V$ and $V_{ref} = 10V$.

Solution

The ramp signal rises at a rate of 2V/ms. Therefore, choose a time constant of R_1C to produce a time period of 1.0 ms.

Let $R_1 = 10\ k\Omega$ and $C = 0.1\ \mu F$. We know that $f = \left(\frac{1}{R_1C}\right)\frac{V_i}{V_{ref}}$

Therefore $$f = \frac{1}{(10\times10^3)(0.1\times10^{-6})}\left(\frac{2}{10}\right) = 200\ Hz$$

5.7 BASIC PRINCIPLE OF SINE WAVE OSCILLATORS

The basic structure of sine wave oscillators based on the use of feedback in amplifiers is shown in Fig. 5.16. It consists of an amplifier with gain A and a frequency selective feedback network (having inductor or capacitive components) with the transfer ratio β. It may be noted that the loop is incomplete as the terminal 2 is not connected to terminal 1. To understand the operation of the circuit, consider the situation where an input signal v_i is applied at the input terminal 1 of the amplifier, so that the output $v_o = A\, v_i$. The feedback signal v_f at terminal 2, therefore is $v_f = A\beta\, v_1$. The quantity Aβ, therefore, represents the loop gain of the system. If the values of A and β are adjusted so that Aβ = 1, the feedback signal v_f will be identically equal to the externally applied signal v_i. If the terminal 2 is now connected to terminal 1 and the external signal v_i is removed, the circuit will continue to provide output as the amplifier can not distinguish whether v_i is coming from external source or from the feedback circuit. Thus, output signal can be continuously obtained without any input signal if we can satisfy the condition on the loop gain, that is,

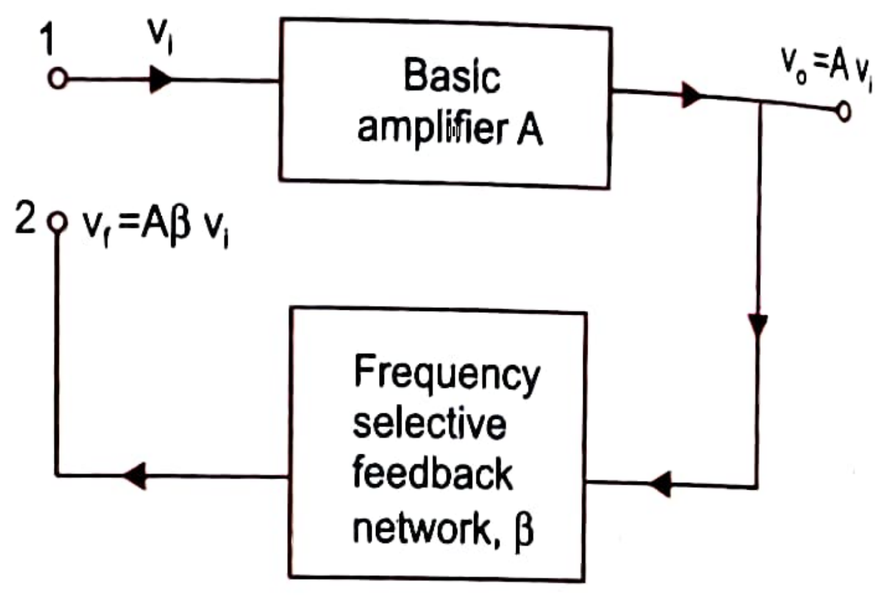


Fig. 5.16 Basic structure of a feedback oscillator

$$A\beta = 1 \tag{5.24}$$

This is called ***Barkhausen criterion*** for oscillations. The condition Aβ = 1 can be satisfied only at one specific frequency, f_o for the given component values. The circuit thus provides output at frequency, f_o where the circuit components meets the condition given by Eq. (5.24). We may rewrite Eq. (5.24) as

$$A(j\omega_o)\, \beta(j\omega_o) = 1\ \angle 0° \tag{5.25}$$

There are infact two conditions in Eq. (5.25), one on phase and other on the magnitude of the loop gain which needs to be simultaneously satisfied to achieve oscillations. Thus, according to Eq. (5.25) the total phase shift of the loop gain should be zero or multiples of 2π and the magnitude of the loop gain, Aβ should be equal to unity. That is

$$|A\beta| = 1 \tag{5.26}$$

$$\angle A\beta = 0° \text{ or multiples of } 2\pi \tag{5.27}$$

The condition |Aβ| = 1 is usually difficult to maintain in the circuit as the values of A and β vary due to temperature variations, aging of components, change of supply voltage etc. If |Aβ| becomes less than unity, the feedback signal v_f goes on reducing in each feedback cycle and the oscillations will die down eventually. In order to ensure that the circuit sustains oscillations inspite of variations, the circuit is designed so that |Aβ| is slightly greater than unity. Now, the output amplitude will go on increasing with every feedback cycle. The signal, however, can not go on increasing and gets limited due to the non-linearity of the device, that is as the transistor enters into saturation. Thus it is the non-linearity of the transistor because of which the sustained oscillations can be achieved. The value of Aβ is usually kept greater by about 1 to 5% to ensure that |Aβ| does not fall below unity. In explaining the principle of oscillation

in Fig. 5.14, we had assumed that we first connect a signal source to start the oscillations and later remove it. In a practical oscillator, however, it is not done so. The output waveform is obtained as soon as power is turned on. Actually, there is noise signal always present at the input (i.e. base) of the transistor due to temperature (called Johnson's noise) or variation in the carrier concentration (Schottky noise). The noise signal at the frequency at which the circuit satisfies the condition $|A\beta| = 1$ is picked up and amplified. Since $|A\beta| > 1$ in the circuit, the output signal goes on increasing until it is limited by the onset of non-linearity of the transistor (as transistor enters into saturation) as shown in Fig. 5.15.

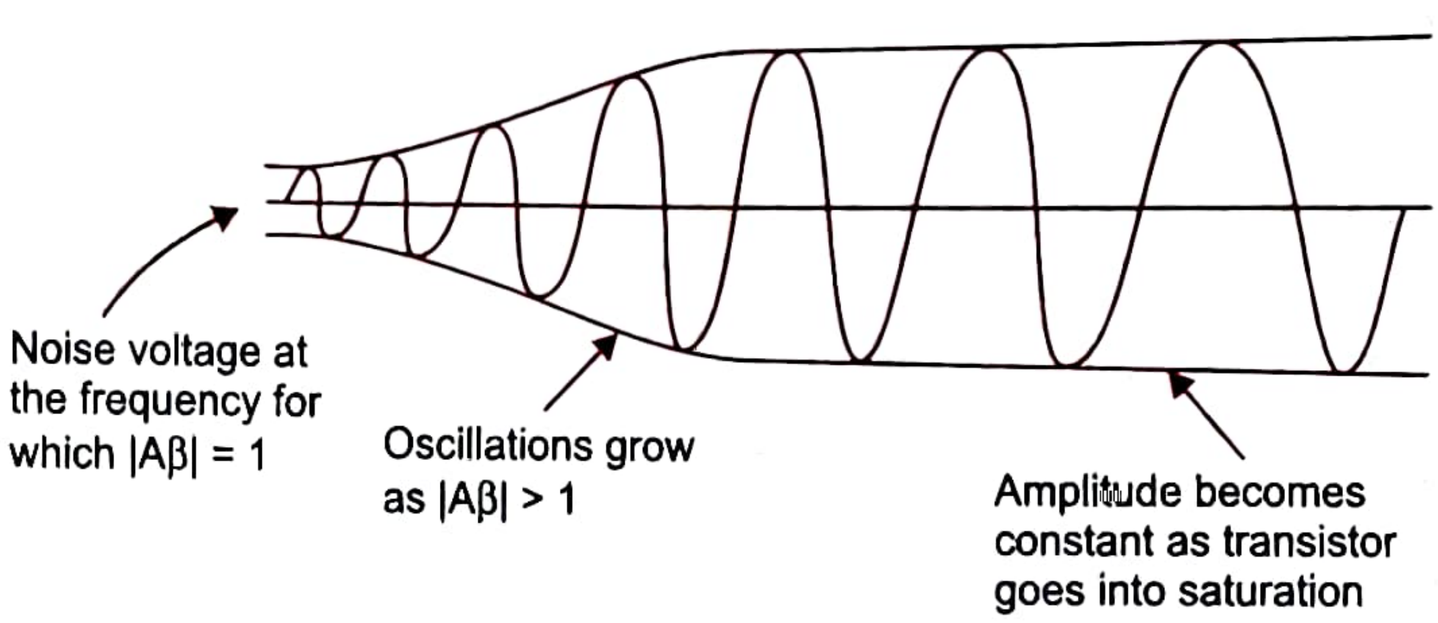


Fig. 5.17 Showing constant output amplitude as transistor goes into saturation ($|A\beta| > 1$)

There are different types of sine-wave oscillators available according to the range of frequency. The RC-phase shift oscillators can provide frequencies varying from a few hertz to several hundred kHz. LC oscillators are suitable for high frequencies up to hundreds of MHz. Here we will discuss only two types of audio frequency RC phase shift oscillators.

RC-Phase Shift Oscillator

The circuit of an RC-phase shift oscillator is shown in Fig. 5.16 (a). The op-amp is used in the inverting mode and therefore provides 180° phase shift. The additional phase of 180° is provided by the RC feedback network to obtain a total phase shift of 360°. The feedback network consists of three identical RC stages. Each of the RC stage provides a 60° phase shift so that the total phase shift due to feedback network is 180°. It is not necessary that all the three RC sections are identical so long the total phase shift is 180°. However, if we use non-identical stages, it is possible that the total phase shift is 180° for more than one frequency. This phenomenon can lead to undesirable inter-modal oscillations.

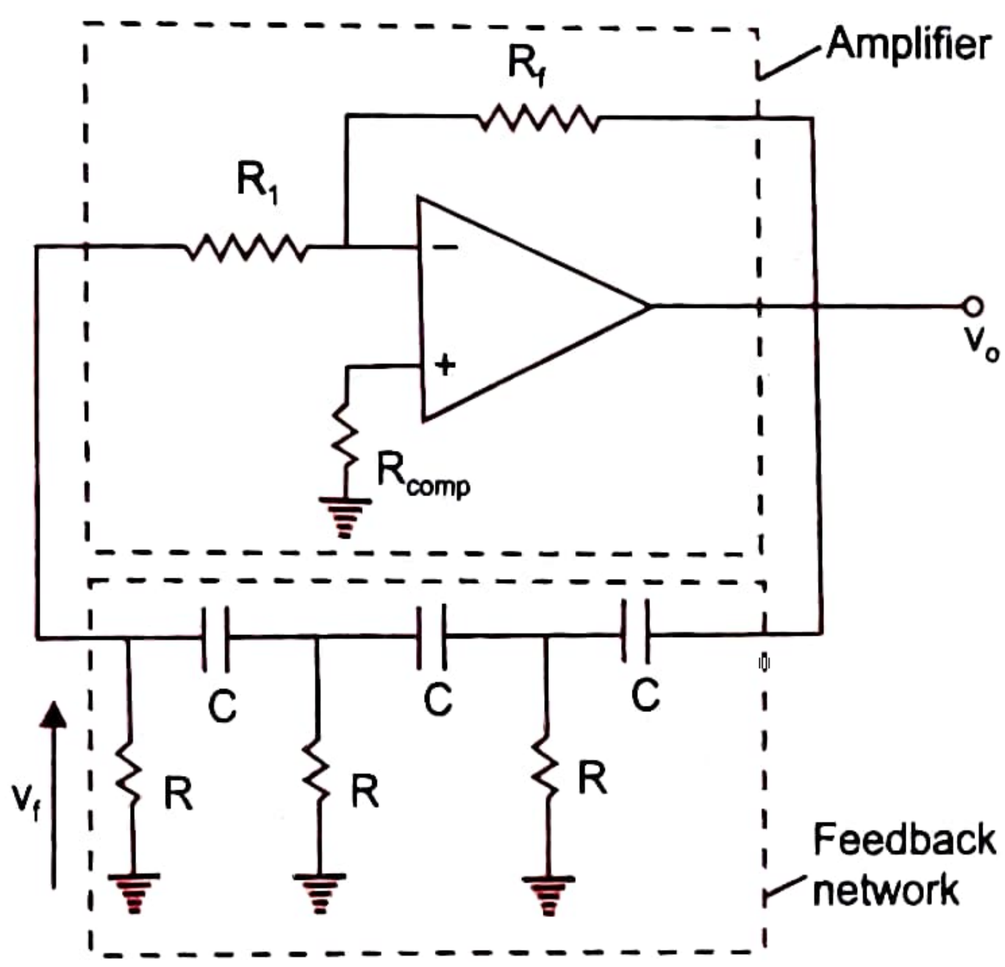


Fig. 5.18 (a) Phase shift oscillator

The feedback factor β of the RC network can be calculated by writing the KVL equations from Fig. 5.16 (b).

$$I_1\left(R+\frac{1}{sC}\right)-I_2R = V_o \qquad (5.28)$$

$$-I_1R+I_2\left(2R+\frac{1}{sC}\right)-I_3R = 0 \qquad (5.29)$$

$$0-I_2R+I_3\left(2R+\frac{1}{sC}\right) = 6 \qquad (5.30)$$

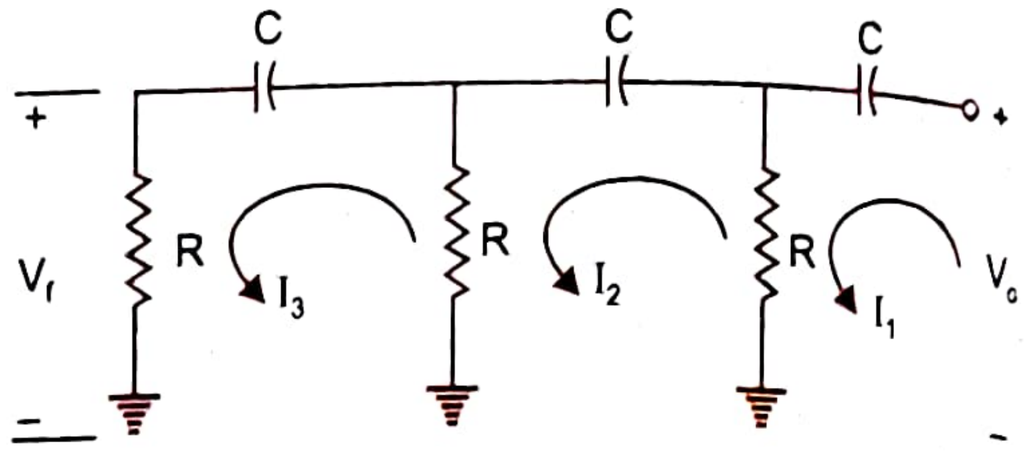


Fig. 5.18 (b) Calculating β from the phase shift network

and $$V_f = I_3R \qquad (5.31)$$

Solving Eqs. (5.28), (5.29) and (5.30) for I_3, we get

$$I_3 = \frac{V_oR^2s^3C^3}{1+5sRC+6s^2C^2R^2+s^3C^3R^3} \qquad (5.32)$$

and $$V_f = I_3R = \frac{V_oR^3s^3C^3}{1+5sRC+6s^2C^2R^2+s^3C^3R^3} \qquad (5.33)$$

$$= \frac{1}{1+\frac{6}{sRC}+\frac{5}{s^2C^2R^2}+\frac{1}{s^3C^3R^3}} \qquad (5.34)$$

Replacing $s = j\omega$, $s^2 = -\omega^2$ and $s^3 = -j\omega^3$, we get

$$\beta = \frac{1}{1-\frac{6}{j\omega RC}-\frac{5}{\omega^2R^2C^2}+\frac{1}{j\omega^3R^3C^3}} \qquad (5.35)$$

$$= \frac{1}{(1-5\alpha^2)+j\alpha(6-\alpha^2)} \qquad (5.36)$$

where $$\alpha = \frac{1}{\omega RC} \qquad (5.37)$$

For $A\beta = 1$, β should be real, that is the imaginary term in Eq. (5.36) must be zero. Thus

$$\alpha\,(6-\alpha^2) = 0 \qquad (5.38)$$

or, $$\alpha^2 = 6$$

$$\alpha = \sqrt{6}$$

That is, $$\frac{1}{\omega RC} = \sqrt{6}$$

The frequency of oscillation, f_o, is therefore given by

$$f_o = \frac{1}{2\pi\,RC\,\sqrt{6}} \qquad (5.39)$$

Putting $\alpha^2 = 6$ in Eq. (5.36), we get

$$\beta = -\frac{1}{29} \tag{5.40}$$

The negative sign indicates that the feedback network produces a phase shift of 180°.

So, $$|\beta| = \frac{1}{29}$$

Since $$|A\beta| \geq 1$$

Therefore, for sustained oscillations,

$$|A| \geq 29 \tag{5.41}$$

That is the gain of the inverting op-amp should be atleast 29, or $R_f = 29\ R_1$. The gain A_v is kept greater than 29 to ensure that variations in circuit parameters will not make $|A_v \beta| < 1$, otherwise oscillations will die out.

For low frequencies (< 1 kHz), op-amp 741 may be used, however, for high frequencies, LM 318 or LF 351 should be used.

Example 5.5

Design a phase shift oscillator of Fig. 5.17 to oscillate at 100 Hz.

Solution

Let $C = 0.1\ \mu F$. Then from Eq. (5.25)

$$R = \frac{1}{\sqrt{6}\ 2\pi (10^{-7})(100)} = 6.49\ k\Omega$$

Use $R = 6.5\ k\Omega$

To prevent loading of the amplifier by RC network, $R_1 \leq 10\ R$

Therefore, let $R_1 = 10\ R = 65\ k\Omega$

Since $R_f = 29\ R_1$

$R_f = 1885\ k\Omega$

Wien Bridge Oscillator

Another commonly used audio frequency oscillator is a Wien bridge oscillator. The circuit is shown in Fig. 5.19. It may be noted that the feedback signal in this circuit is connected to the non-inverting (+) input terminal so that the op-amp is working as a non-inverting amplifier. Therefore, the feedback network need not provide any phase shift. The circuit can be viewed as a Wien bridge with a series RC network in one arm and a parallel RC network in the adjoining arm. Resistors R_1 and R_F are connected in the remaining two arms. The condition of zero phase shift around the circuit is achieved by balancing the bridge.

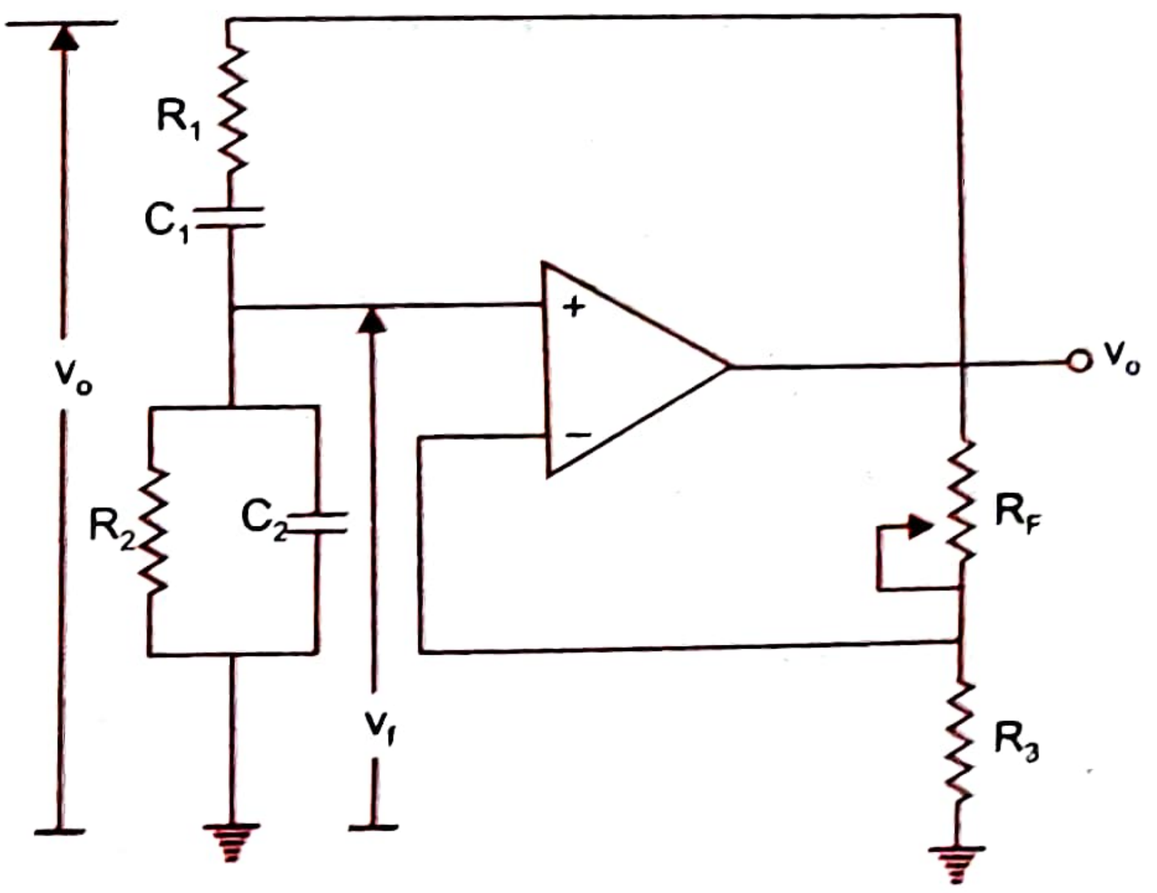


Fig. 5.19 Wien bridge oscillator

The circuit has been redrawn to show the bridge network in Fig. 5.20. The output ac signal of the op-amp amplifier is fed back to point A of the bridge. The feedback signal, V_f across the parallel combination R_2C_2 is applied to the non-inverting input terminal of the op-amp. The gain of the op-amp amplifier is

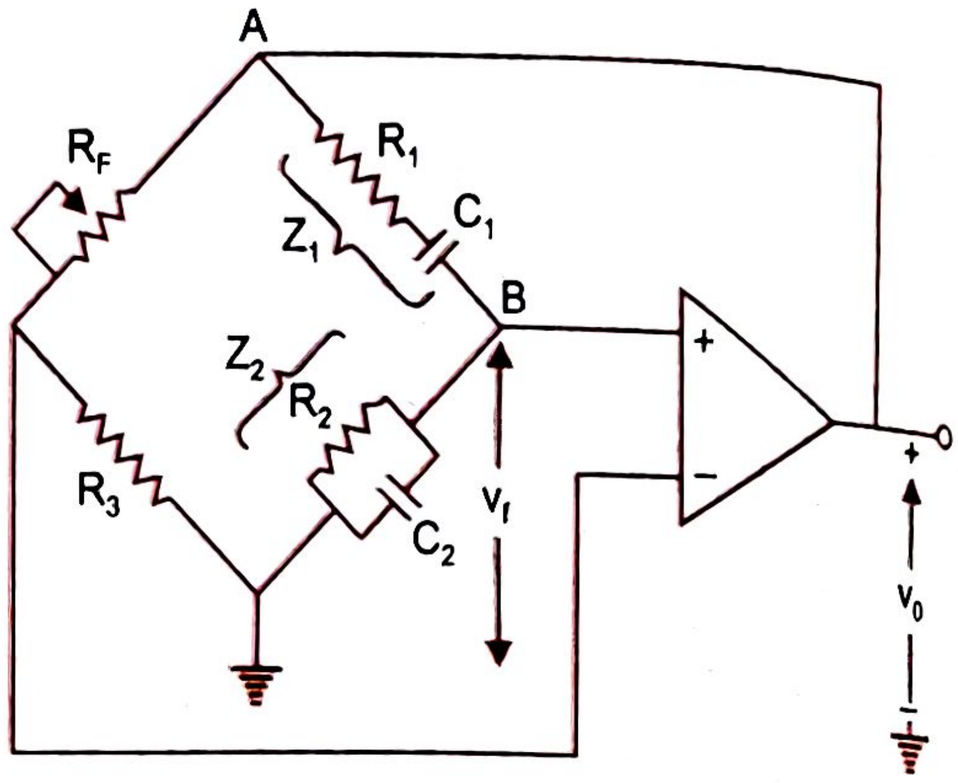


Fig. 5.20 Wien bridge oscillator showing the bridge network

$$A = 1 + \frac{R_F}{R_3} \tag{5.42}$$

and feedback factor, β from Fig. 5.18 is

$$\beta = \frac{V_f}{V_o} = \frac{Z_2}{Z_1 + Z_2} \tag{5.43}$$

where $$Z_1 = R_1 + \frac{1}{sC_1} = \frac{sR_1C_1 + 1}{sC_1} \tag{5.44}$$

$$Z_2 = \frac{R_2}{1 + sR_2C_2} \tag{5.45}$$

Putting the values of Z_1 and Z_2 in Eq.(5.43), we get

$$\beta = \frac{R_2/(1 + R_2C_2s)}{\frac{1 + sR_1C_1}{sC_1} + \frac{R_2}{1 + sR_2C_2}} \tag{5.46}$$

$$= \frac{sR_2C_1}{1 + s(R_1C_1 + R_2C_2 + R_2C_1) + s^2R_1R_2C_1C_2} \tag{5.47}$$

Putting $s = j\omega$,

$$\beta = \frac{j\omega R_2C_1}{1 + j\omega(R_1C_1 + R_2C_2 + R_2C_1) - \omega^2R_1R_2C_1C_2} \tag{5.48}$$

In order β to be a real quantity

$$1 - \omega^2R_1R_2C_1C_2 = 0$$

Thus, the frequency of oscillation,

$$f_o = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}} \tag{5.49}$$

and

$$\beta = \frac{R_2C_1}{R_1C_1 + R_2C_2 + R_2C_1} \tag{5.50}$$

For $R_1 = R_2 = R$ and $C_1 = C_2 = C$,

$$f_o = \frac{1}{2\pi RC} \tag{5.51}$$

and

$$\beta = \frac{1}{3} \tag{5.52}$$

Since $|A\beta| \geq 1$ for sustained oscillations,

$$|A| \geq 3$$

Since

$$A = 1 + \frac{R_F}{R_3}$$

$$3 = 1 + \frac{R_F}{R_3}$$

or,

$$R_F = 2R_3 \tag{5.53}$$

If the gain $|A| > 3$, sometimes oscillations keep growing and it may clip the output sinewave. This problem is eliminated by a practical Wien bridge oscillator with adaptive negative feedback as shown in Fig. 5.21. In this circuit, resistor R_4 is initially adjusted to give a gain so that oscillations start. The output signal grows in amplitude until the voltage across R_3 approaches the cut-in voltage of the diode. As the diodes begin to turn-on (one for the positive half cycle and the other for the negative half cycle), the effective feedback resistance R_F decreases because the diode is in parallel with the resistance R_3. This will reduce the gain of the amplifier which in turn lowers the output amplitude. Hence sustained oscillations can be obtained. Further, if the output signal falls, the diodes would begin to turn-off thereby increasing R_F which in turn increases gain.

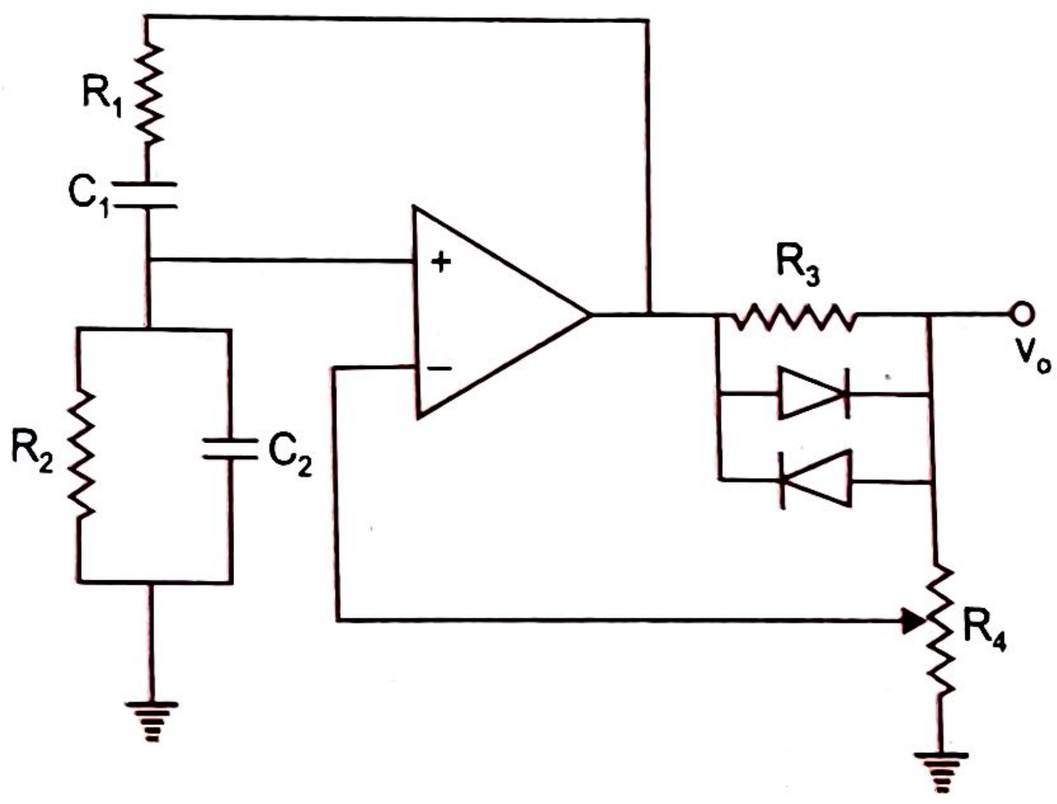


Fig. 5.21 Practical Wien bridge oscillator with adaptive negative feedback

The two op-amp RC oscillator circuits studied are suitable for the frequency range of 10 Hz to 100 kHz (maximum 1 MHz). The size of R and C components becomes very large for generating low frequencies. Thus, the low frequency limit is dictated by the size of passive components required. The upper frequency limit is governed by the frequency response and slew rate limit of the op-amp used. For generating high frequencies in the RF range, the oscillator circuits are usually designed using BJT and LC tuned circuits or crystal oscillators.

LC Oscillators

For generating high frequency sine waves in the RF range, LC tuned circuits are used. The most commonly used LC oscillators are Colpitts oscillator and Hartley oscillator which are discussed here.

7

ACTIVE FILTERS

7.1 INTRODUCTION

Electric filters are used in circuits which require the separation of signals according to their frequencies. Filters are widely used in communication and signal processing and in one form or another in almost all sophisticated electronic instruments. Such filters can be built from, (i) passive RLC components, (ii) crystals or (iii) resistors, capacitors and op-amps (active filters). In this chapter, we are discussing (i) RC active filters and (ii) switched capacitor filters. Further, active filters in its low-pass, high-pass, band-pass, band elimination configura-tion and state variable filter have been discussed.

7.2 RC ACTIVE FILTERS

A frequency selective electric circuit that passes electric signals of specified band of frequencies and attenuates the signals of frequencies outside the band is called an electric filter. Filters may be analog or digital. Our point of discussion, in this chapter, will be analog filters.

The simplest way to make a filter is by using passive components (resistors, capacitors, inductors). This works well for high frequencies, that is, radio frequencies. However, at audio frequencies, inductors become problematic, as the inductors become large, heavy and expensive. For low frequency application, more number of turns of wire must be used which in turn adds to the series resistance degrading inductor's performance, i.e. low Q, resulting in high power dissipation.

The active filters overcome the aforementioned problems of the passive filters. They use op-amp as the active element, and resistors and capacitors as the passive elements. The active filters, by enclosing a capacitor in the feedback loop, avoid using inductors. In this way, inductorless active RC filters can be obtained. Op-amps filters have the advantage that they can provide gain. Thus, the input signal is not attenuated as in the case of passive filters. Also, as op-amp is used in non-inverting configuration, it offers high input impedance and low output impedance. This will improve the load drive capacity and the load is isolated from the frequency determining network. Because of the high input impedance of the op-amp, large value resistors can be used, thereby reducing the value (size and cost) of the capacitors required in the design.

The active filters have their limitation too. High frequency response is limited by the gain-bandwidth (GBW) product and slew rate of the op-amp. Moreover, the high frequency active filters are more expensive than the passive filters. The passive filter in high frequency range is a more economic choice for applications.

The most commonly used filters are:

Low Pass Filter (LPF)
High Pass Filter (HPF)
Band Pass Filter (BPF)
Band Reject Filter (also called Band Stop Filter) (BSF)

The frequency response of these filters is shown in Fig. 7.1, where dashed curve indicates the ideal response and solid curve shows the practical filter response. It is not possible to achieve ideal characteristics. However, with special design techniques it is possible to closely approximate the ideal response.

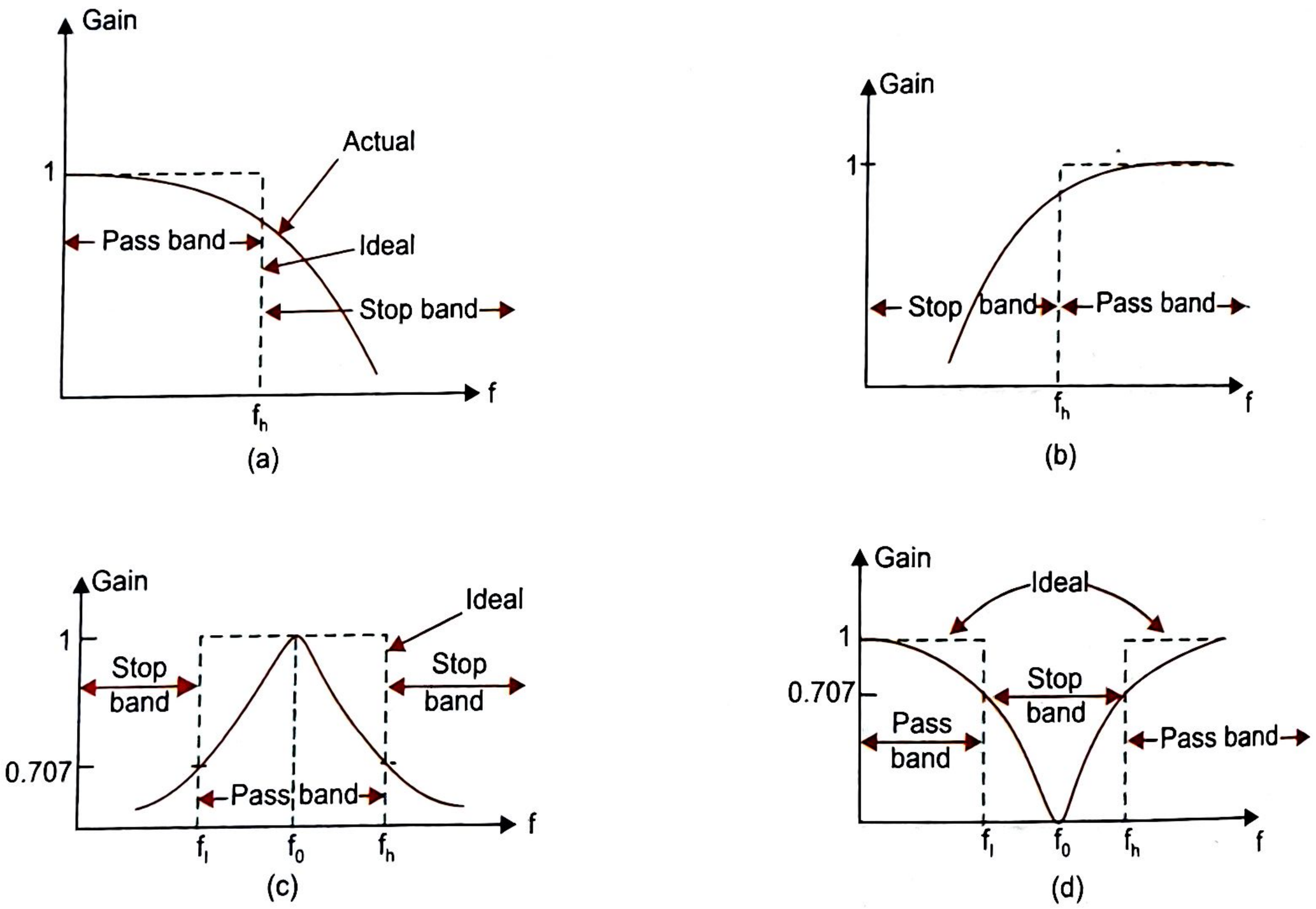


Fig. 7.1 Frequency response of filters, (a) Low-pass, (b) High-pass, (c) Band-pass, (d) Band-reject

Active filters are typically specified by the voltage transfer function,

$$H(s) = \frac{V_o(s)}{V_i(s)}$$

Under steady state conditions (i.e., $s = j\omega$)

$$H(j\omega) = |H(j\omega)| e^{j\phi(\omega)} \tag{7.1}$$

where $|H(j\omega)|$ is the magnitude or the gain function and $\phi(\omega)$ is the phase function. Usually the magnitude response is given in dB as

$$20 \log |H(j\omega)| \tag{7.2}$$

and the phase response is given in degrees as

$$-\phi(\omega) \times 57.296 \text{ degrees} \tag{7.3}$$

Sometimes, active filters are specified by a loss function $V_i(s)/V_o(s)$. The use of loss function is a carry over from passive filter design.

7.2.1 First Order Low Pass Filter

Active filters may be of different orders and types. A first order filter consists of a single RC network connected to the (+) input terminal of a non-inverting op-amp amplifier and is shown in Fig. 7.2 (a). Resistors R_i and R_F determine the gain of the filter in the pass band.

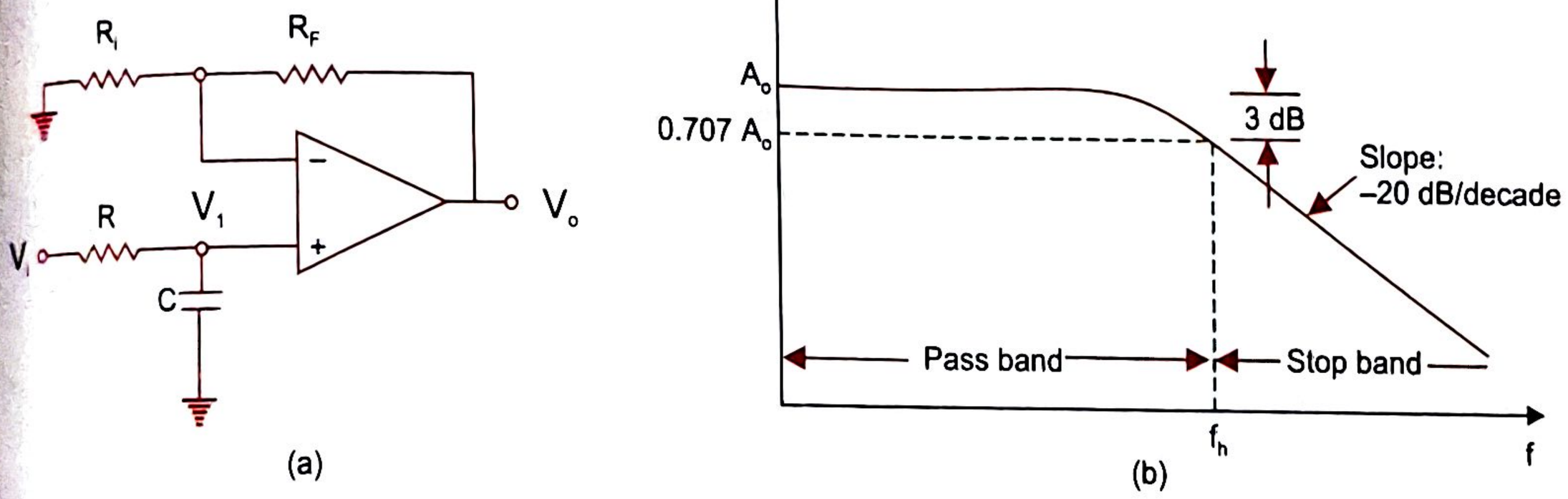


Fig. 7.2 (a) First order low-pass filter, (b) Frequency response

The voltage V_1 across the capacitor C in the s-domain is

$$V_1(s) = \frac{\frac{1}{sC}}{R + \frac{1}{sC}} V_i(s)$$

So,

$$\frac{V_1(s)}{V_i(s)} = \frac{1}{RCs + 1} \tag{7.4}$$

where $V(s)$ is the Laplace transform of v in time domain.

The closed loop gain A_o of the op-amp is,

$$A_o = \frac{V_o(s)}{V_1(s)} = \left(1 + \frac{R_F}{R_i}\right) \tag{7.5}$$

So, the overall transfer function from Eqs. (7.4) and (7.5) is

$$H_{LP}(s) = \frac{V_o(s)}{V_i(s)} = \frac{V_o(s)}{V_1(s)} \cdot \frac{V_1(s)}{V_i(s)} = \frac{A_o}{RCs + 1} \tag{7.6}$$

Let

$$\omega_h = \frac{1}{RC} \tag{7.7}$$

Therefore, $$H_{LP}(s) = \frac{V_o(s)}{V_i(s)} = \frac{A_o}{\frac{s}{\omega_h} + 1} = \frac{A_o \omega_h}{s + \omega_h} \quad (7.8)$$

This is the standard form of the transfer function of a first order low pass system. To determine the frequency response, put $s = j\omega$ in Eq. (7.8). Therefore, we get

$$H_{LP}(j\omega) = \frac{A_o}{1 + j\omega RC} = \frac{A_o}{1 + j(f/f_h)} \quad (7.9)$$

where $$f_h = \frac{1}{2\pi RC} \text{ and } f = \frac{\omega}{2\pi}$$

At very low frequency, i.e. $f << f_h$

$$|H_{LP}(j\omega)| \simeq A_o \quad (7.10)$$

At $f = f_h$,

$$|H_{LP}(j\omega)| = \frac{A_o}{\sqrt{2}} = 0.707\, A_o \quad (7.11)$$

At very high frequency i.e. $f >> f_h$

$$|H_{LP}(j\omega)| << A_o \simeq 0 \quad (7.12)$$

The frequency response of the first order low pass filter is shown in Fig. 7.2 (b). It has the maximum gain, A_o at $f = 0$ Hz. At f_h the gain falls to 0.707 time (i.e. –3 dB down) the maximum gain (A_o). The frequency range from 0 to f_h is called the pass band. For $f > f_h$ the gain decreases at a constant rate of –20 dB/decade. That is, when the frequency is increased ten times (one decade), the voltage gain is divided by ten or in terms of dBs, the gain decreases by 20 dB (= 20 log 10). Hence, gain rolls off at the rate of 20 dB/decade or 6 dB/octave after frequency, f_h. The frequency range $f > f_h$ is called the stop band. Obviously, the low pass filter characteristics obtained is not an ideal one as the rate of decay is small for the first order filter.

7.2.2 Second Order generalised Active Filter (Sallen-key filter)

An improved filter response can be obtained by using a second order active filter. A second order filter consists of two RC pairs and has a roll-off rate of – 40 dB/decade. A general second order filter (Sallen-Key filter) is shown in Fig. 7.3. The results derived here can be used for analysing low pass and high pass filters.

The op-amp is connected as non-inverting amplifier and hence,

$$v_o = \left(1 + \frac{R_F}{R_i}\right) v_B = A_o v_B \quad (7.13)$$

where $$A_o = 1 + \frac{R_F}{R_i} \quad (7.14)$$

and v_B is the voltage at node B.

Kirchhoff's current law (KCL) at node A gives

$$v_i Y_1 = v_A(Y_1 + Y_2 + Y_3) - v_o Y_3 - v_B Y_2$$

$$= v_A(Y_1 + Y_2 + Y_3) - v_o Y_3 - \frac{v_o Y_2}{A_o} \quad (7.15)$$

where v_A is the voltage at node A.

KCL at node B gives,

$$v_A Y_2 = v_B(Y_2 + Y_4) = \frac{v_o(Y_2 + Y_4)}{A_o}$$

$$v_A = \frac{v_o(Y_2 + Y_4)}{A_o Y_2} \quad (7.16)$$

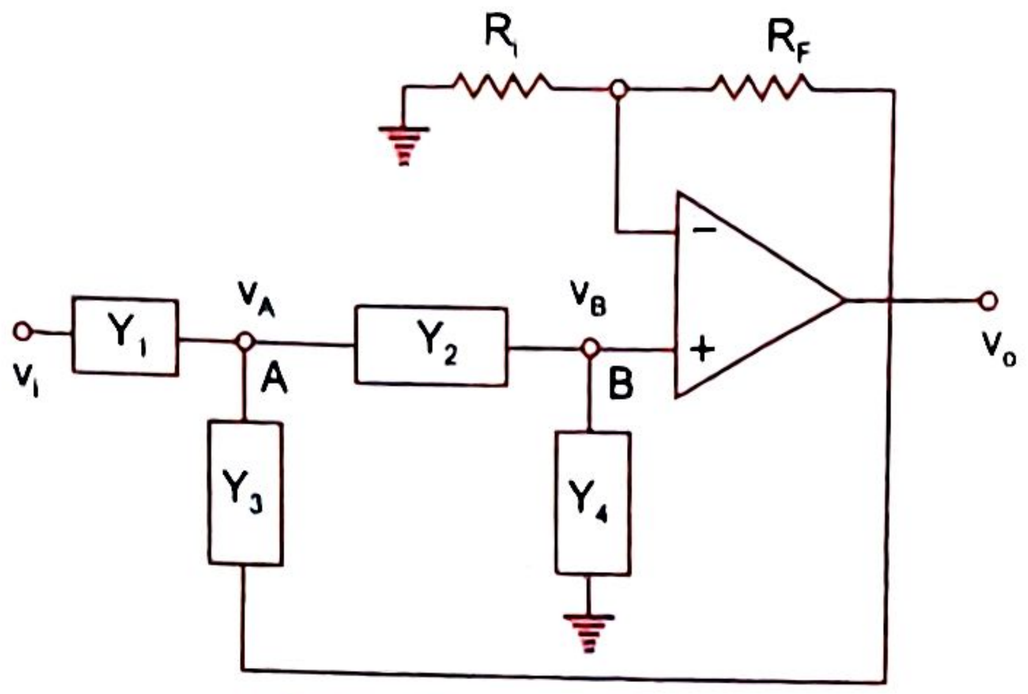


Fig. 7.3 Sallen-Key filter
(General second order filter)

Substituting Eq. (7.16) in Eq. (7.15) and after simplification, we get the voltage gain as

$$\frac{v_o}{v_i} = \frac{A_o Y_1 Y_2}{Y_1 Y_2 + Y_4(Y_1 + Y_2 + Y_3) + Y_2 Y_3 (1 - A_o)} \quad (7.17)$$

To make a low pass filter, choose, $Y_1 = Y_2 = 1/R$ and $Y_3 = Y_4 = sC$ as shown in Fig. 7.4. For simplicity, equal components have been used.

From Eq. (7.17), we get the transfer function $H(s)$ of a low pass filter as,

$$H(s) = \frac{A_o}{s^2 C^2 R^2 + sCR(3 - A_o) + 1} \quad (7.18)$$

This is to note that from Eq. (7.18), $H(0) = A_o$ for $s = 0$ and $H(\infty) = 0$ for $s = \infty$ and obviously the configuration is for low pass active filter. It may be noted that for minimum dc offset $R_i R_F / (R_F + R_i) = R + R = 2R$ should be satisfied.

Second order physical systems have been studied extensively since long back and their step response, damping coefficient and its cause and effect relationship are known. We shall exploit those ideas in case of second order RC active filter. The transfer function of low pass second order system (electrical, mechanical, hydraulic or chemical) can be written as,

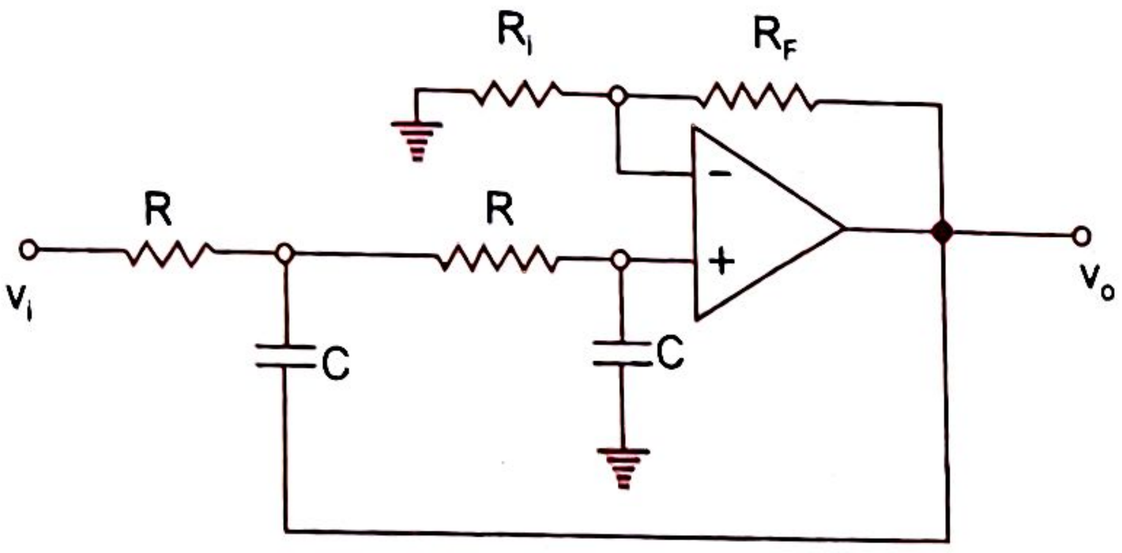


Fig. 7.4 Second order low-pass filter

$$H_{LP}(s) = \frac{A_o \omega_h^2}{s^2 + \alpha \omega_h s + \omega_h^2} \quad (7.19)$$

where A_o = the gain

ω_h = upper cut-off frequency in radians/second

α = damping coefficient

Comparing Eq. (7.18) and Eq. (7.19), we get,

$$\omega_h = \frac{1}{RC} \tag{7.20}$$

$$\alpha = (3 - A_o) \tag{7.21}$$

That is, the value of the damping coefficient α for low pass active RC filter can be determined by the value of A_o chosen.

Putting $s = j\omega$ in Eq. (7.19), we get

$$H_{LP}(j\omega) = \frac{A_o}{(j\omega/\omega_h)^2 + j\alpha(\omega/\omega_h) + 1} \tag{7.22}$$

the normalized expression for low pass filter is

$$H_{LP}(j\omega) = \frac{A_o}{s_n^2 + \alpha s_n + 1} \tag{7.23}$$

where normalized frequency $s_n = j\left(\frac{\omega}{\omega_h}\right)$

The expression of magnitude in dB of the transfer function is,

$$20 \log |H(j\omega)| = 20 \log \left| \frac{A_o}{1 + j\alpha(\omega/\omega_h) + (j\omega/\omega_h)^2} \right|$$

$$= 20 \log \frac{A_o}{\sqrt{\left(1 - \frac{\omega^2}{\omega_h^2}\right)^2 + \left(\alpha \frac{\omega}{\omega_h}\right)^2}} \tag{7.24}$$

The frequency response for different values of α is shown in Fig. 7.5. It may be seen that for a heavily damped filter ($\alpha > 1.7$), the response is stable. However, the roll-off begins very

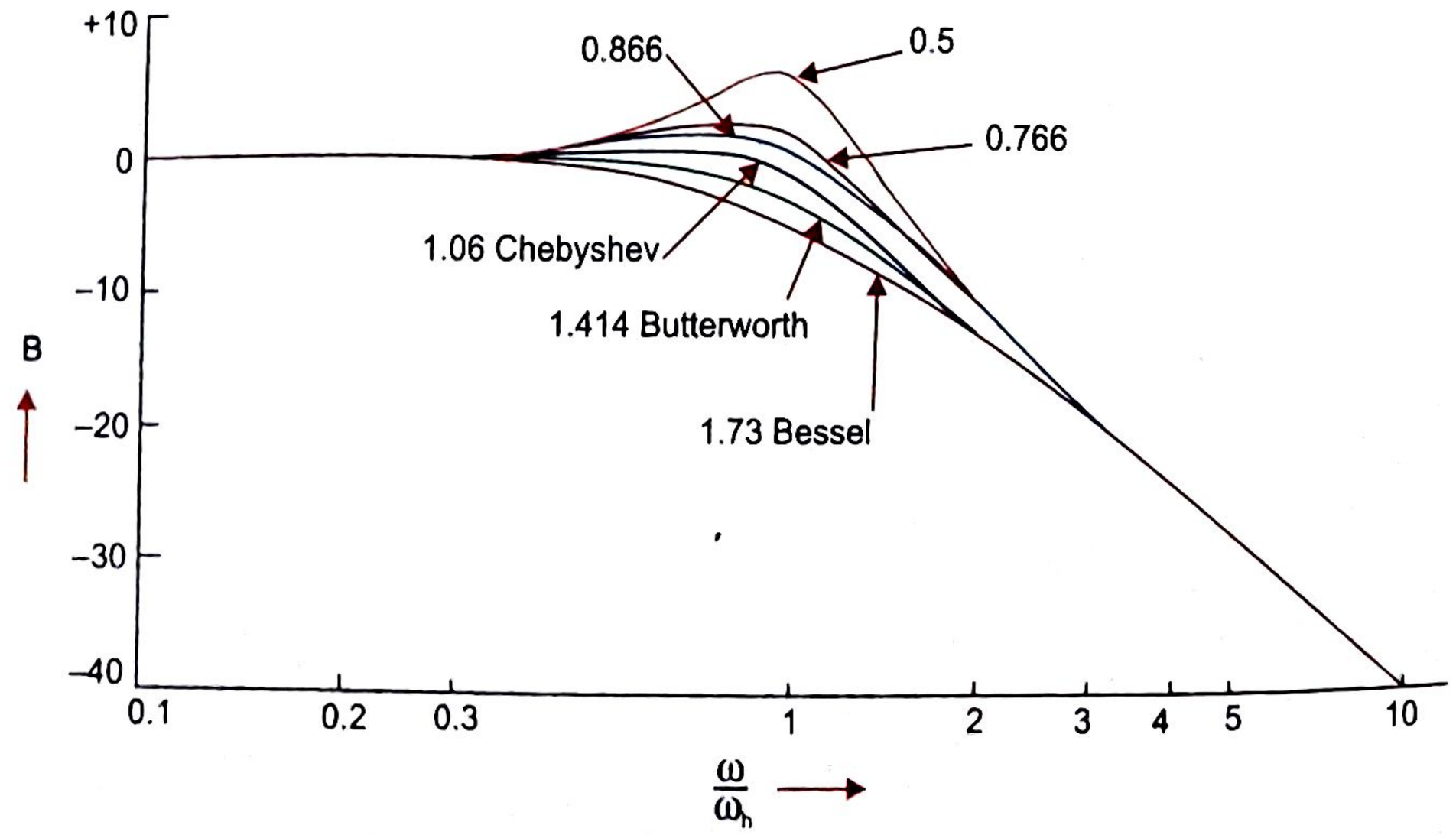


Fig. 7.5 Second order low-pass active filter response for different damping (unity gain $A_o = 1$)

early to the pass band. As α is reduced, the response exhibits overshoot and ripple begins to appear at the early stage of pass band. If α is reduced too much, the filter may become oscillatory. The flattest pass band occurs for damping coefficient of 1.414. This is called a ***Butterworth filter***. Audio filters are usually Butterworth. The ***Chebyshev filters*** are more lightly damped, that is, the damping coefficient α is 1.06. However, this increases overshoot and ringing occurs deteriorating the pulse response. The advantage, however, is a faster initial roll-off compared to Butterworth. A ***Bessel filter*** is heavily damped and has a damping coefficient of 1.73. This gives better pulse response, however, causes attenuation in the upper end of the pass band.

We shall discuss only Butterworth filter in this text as it has maximally flat response with damping coefficient $\alpha = 1.414$. From Eq. 7.24, with $\alpha = 1.414$, we get

$$20 \log |H_{LP}(j\omega)| = 20 \log \left| \frac{V_o}{V_i} \right| = 20 \log \frac{A_o}{\sqrt{1 + \left(\frac{\omega}{\omega_h} \right)^4}} \tag{7.25}$$

Hence for n-th order generalized low-pass Butterworth filter, the normalized transfer function for maximally flat filter can be written as

$$\left| \frac{H_{LP}(j\omega)}{A_o} \right| = \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_h} \right)^{2n}}} \tag{7.26}$$

7.2.3 Higher Order Low Pass Filter

A second order filter can provide –40 dB/decade roll-off rate in the stop band. To match with ideal characteristics, the roll-off rate should be increased by increasing the order of the filter. Each increase in order will produce –20 dB/decade additional increase in roll-off rate, as shown in Fig. 7.6. For n-th order filter the roll-off rate will be $-n \times 20$ dB/decade.

Higher order filters can be built by cascading a proper number of first and second order filters. The transfer function will be of the type,

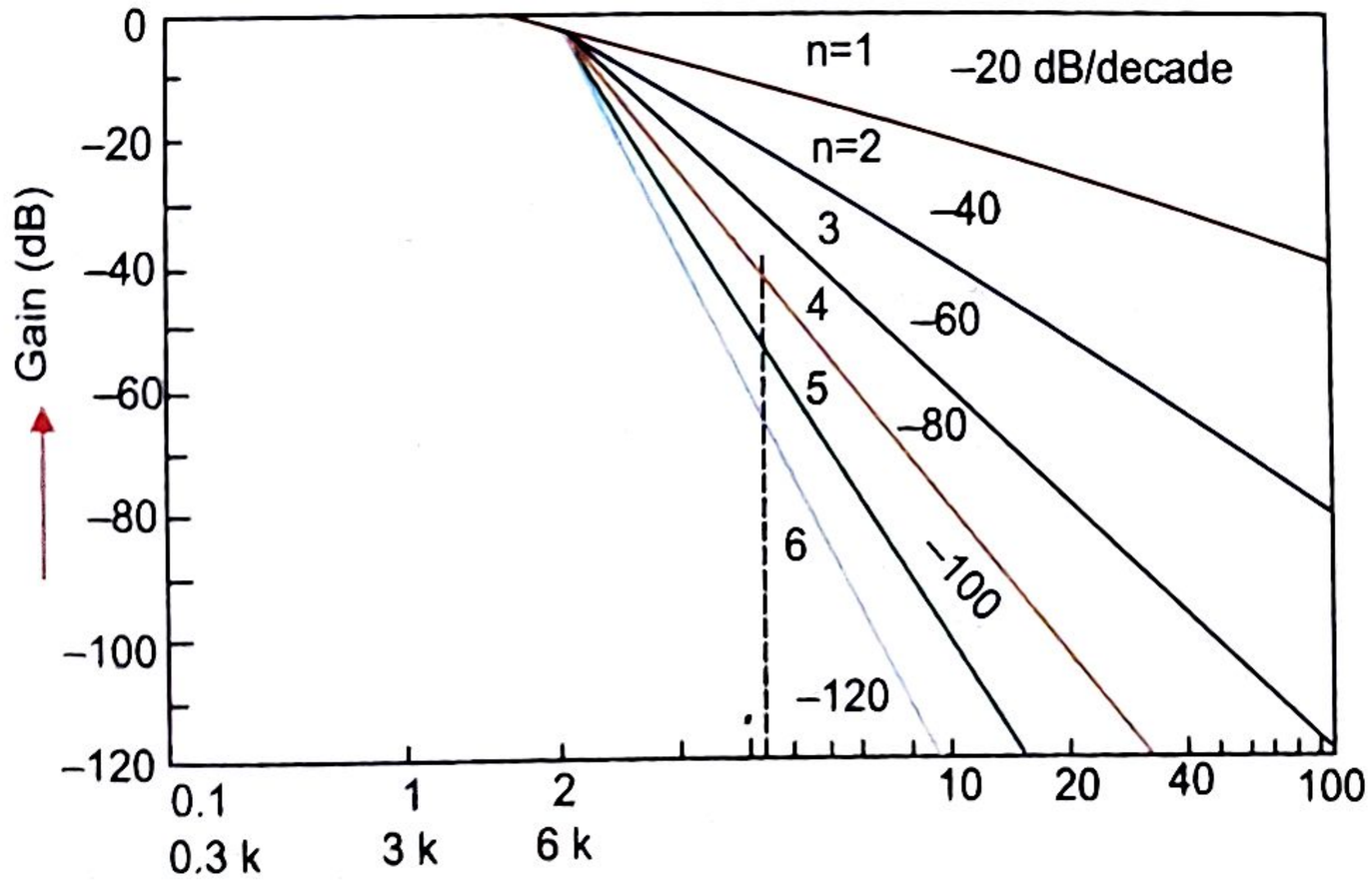


Fig. 7.6 Roll-off rate for different values of n

$$H(s) = \underbrace{\frac{A_{o1}}{s_n^2 + \alpha_1 s_n + 1}}_{\text{second order section}} \cdot \underbrace{\frac{A_{o2}}{s_n^2 + \alpha_2 s_n + 1}}_{\text{another second order section}} \cdot \underbrace{\frac{A_o}{s_n + 1}}_{\text{first order section}}$$

Each term in the denominator has its own damping coefficient and critical frequency. Table 7.1 shows the denominator polynomials upto 8-th order Butterworth filter (see Appendix 7.1).

Table 7.1 Normalized Butterworth polynomial

Order n	*Factors of polynomials*
1.	$s_n + 1$
2.	$s_n^2 + 1.414\ s_n + 1$
3.	$(s_n + 1)(s_n^2 + s_n + 1)$
4.	$(s_n^2 + 0.765\ s_n + 1)(s_n^2 + 1.848\ s_n + 1)$
5.	$(s_n + 1)(s_n^2 + 0.618\ s_n + 1)(s_n^2 + 1.618\ s_n + 1)$
6.	$(s_n^2 + 0.518\ s_n + 1)(s_n^2 + 1.414\ s_n + 1)(s_n^2 + 1.932\ s_n + 1)$
7.	$(s_n + 1)(s_n^2 + 0.445\ s_n + 1)(s_n^2 + 1.247\ s_n + 1)(s_n^2 + 1.802\ s_n + 1)$
8.	$(s_n^2 + 0.390\ s_n + 1)(s_n^2 + 1.111\ s_n + 1)(s_n^2 + 1.663\ s_n + 1)(s_n^2 + 1.962\ s_n + 1)$

Example 7.1

Design a second order Butterworth low-pass filter having upper cut-off frequency 1 kHz. Then determine its frequency response.

Solution

Given $f_h = 1$ kHz $= 1/2\ \pi\ RC$. Let $C = 0.1\ \mu$F, gives the choice of $R = 1.6\ k\Omega$. From Table 7.1. for $n = 2$, the damping factor $\alpha = 1.414$. Then the pass band gain $A_o = 3 - \alpha = 3 - 1.414 = 1.586$. The transfer function of the normalised second order low-pass Butterworth filter is

$$\frac{1.586}{s_n^2 + 1.414\ s_n + 1}$$

Now $A_o = 1 + R_F/R_i = 1.586 = 1 + 0.586$. Let $R_F = 5.86\ k\Omega$ and $R_i = 10\ k\Omega$. Then we get $A_o = 1.586$. The circuit realized is as in Fig. 7.4 with component values as $R = 1.6\ k\Omega$. $C = 0.1\ \mu$F. $R_F = 5.86\ k\Omega$ and $R_i = 10\ k\Omega$.

For minimum dc offset $R_i \| R_F = 2R$ (at dc condition, capacitors are open) which has not been taken into consideration here, otherwise, we would have to modify the values of R and C accordingly which comes out to be $R = 1.85\ k\Omega$, $C = 0.086\ \mu$F, $R_F = 5.86\ k\Omega$, $R_i = 10\ k\Omega$.

The frequency response data is shown in Table 7.2 using Eq. 7.25 and the frequency range is taken from $0.1\ f_h$ to $10\ f_h$ i.e., 100 Hz to 10 kHz as $f_h = 1$ kHz.

Table 7.2

Frequency, f in Hz	*Gain magnitude in dB 20 log (v_o/v_i)*
100 (0.1 f_h)	4.00
200 (0.2 f_h)	4.00
500 (0.5 f_h)	3.74
1000 (1.0 f_h)	1.00
5000 (5 f_h)	−23.95
10000 (10 f_h)	−35.99

Example 7.2

Design a fourth order Butterworth low-pass filter having upper cut-off frequency 1 kHz.

Solution

The upper cut-off frequency, $f_h = 1$ kHz $= 1/2\pi RC$. Let $C = 0.1$ μF gives the choice of $R = 1.6$ kΩ. From Table 7.1, for $n = 4$, we get two damping factors namely, $\alpha_1 = 0.765$ and $\alpha_2 = 1.848$. Then the pass band gain of two quadratic factors are

$$A_{o1} = 3 - \alpha_1 = 3 - 0.765 = 2.235$$

$$A_{o2} = 3 - \alpha_2 = 3 - 1.848 = 1.152$$

The transfer function of fourth order low-pass Butterworth filter is

$$\frac{2.235}{s_n^2 + 0.765 s_n + 1} \cdot \frac{1.152}{s_n^2 + 1.848 s_n + 1}$$

Now, $$A_{o1} = 1 + \frac{R_{F1}}{R_{i1}} = 2.235 = (1 + 1.235)$$

Let $R_{F1} = 12.35$ kΩ and $R_{i1} = 10$ kΩ, then we get $A_{o1} = 2.235$
Similarly,

$$A_{o2} = 1.152 = 1 + 0.152 = 1 + \frac{R_{F2}}{R_{i2}}$$

Let $R_{F2} = 15.2$ kΩ and $R_{i2} = 100$ kΩ, which gives $A_{o2} = 1.152$.
The circuit realization is shown in Fig. 7.7.

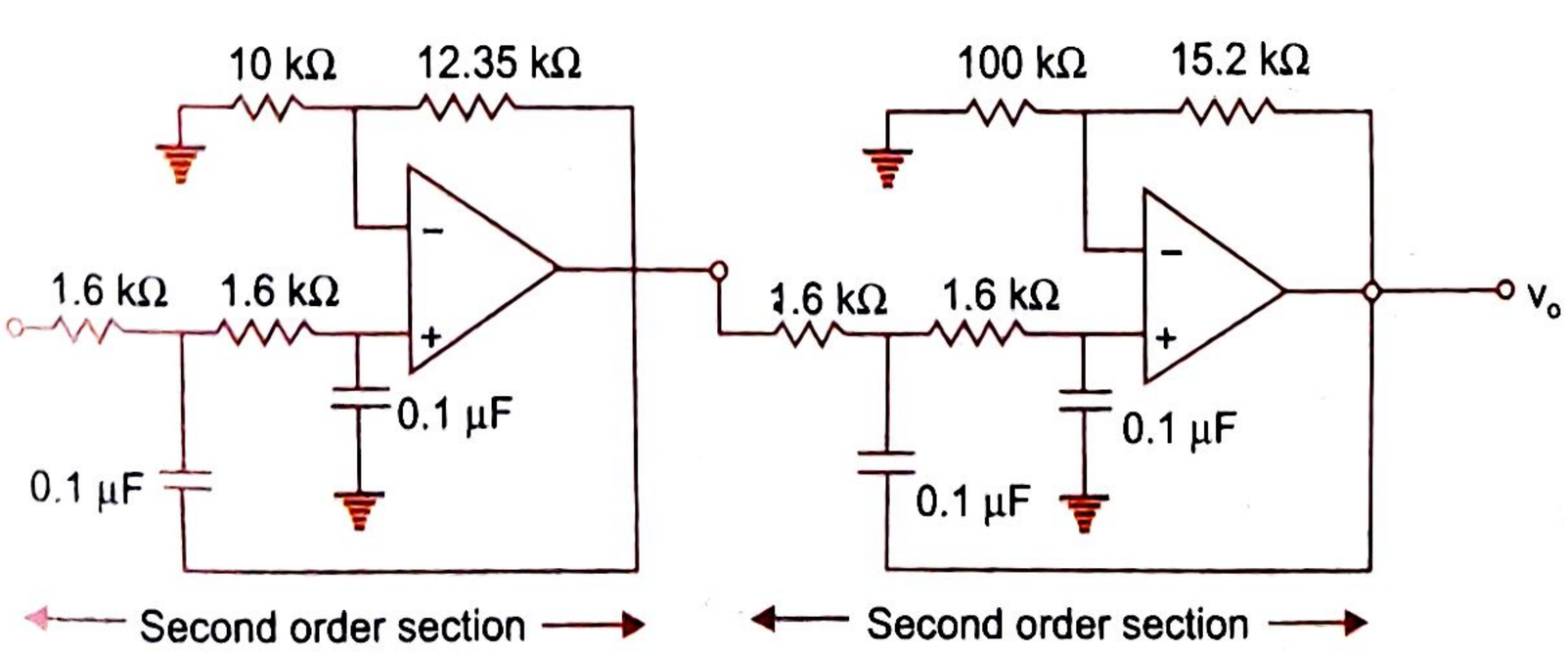


Fig. 7.7 Realization of 4-th order Butterworth low-pass filter

Example 7.3

Determine the order of a low-pass Butterworth filter that is to provide 40 dB attenuation at $\omega_h = 2$.

Solution

Use Eq. 7.26, then

$$20 \log \frac{H(j\omega)}{A_0} = -40 \text{ dB}$$

gives $$\frac{H(j\omega)}{A_0} = 0.01$$

so $$(0.01)^2 = \frac{1}{1+2^{2n}}$$

or, $$2^{2n} = 10^4 - 1$$

Solving for n, we get $n = 6.64$

Since the order of the filter must be an integer so, $n = 7$.

7.2.4 High Pass Active Filter

A high pass filter is the complement of the low pass filter and can be obtained simply by interchanging R and C in the low pass configurations discussed earlier. A first order high pass filter is shown in Fig 7.8. It can be seen that a single RC network is connected to the non-inverting terminal of the op-amp and the gain of the filter is controlled by the feedback network $R_i R_F$.

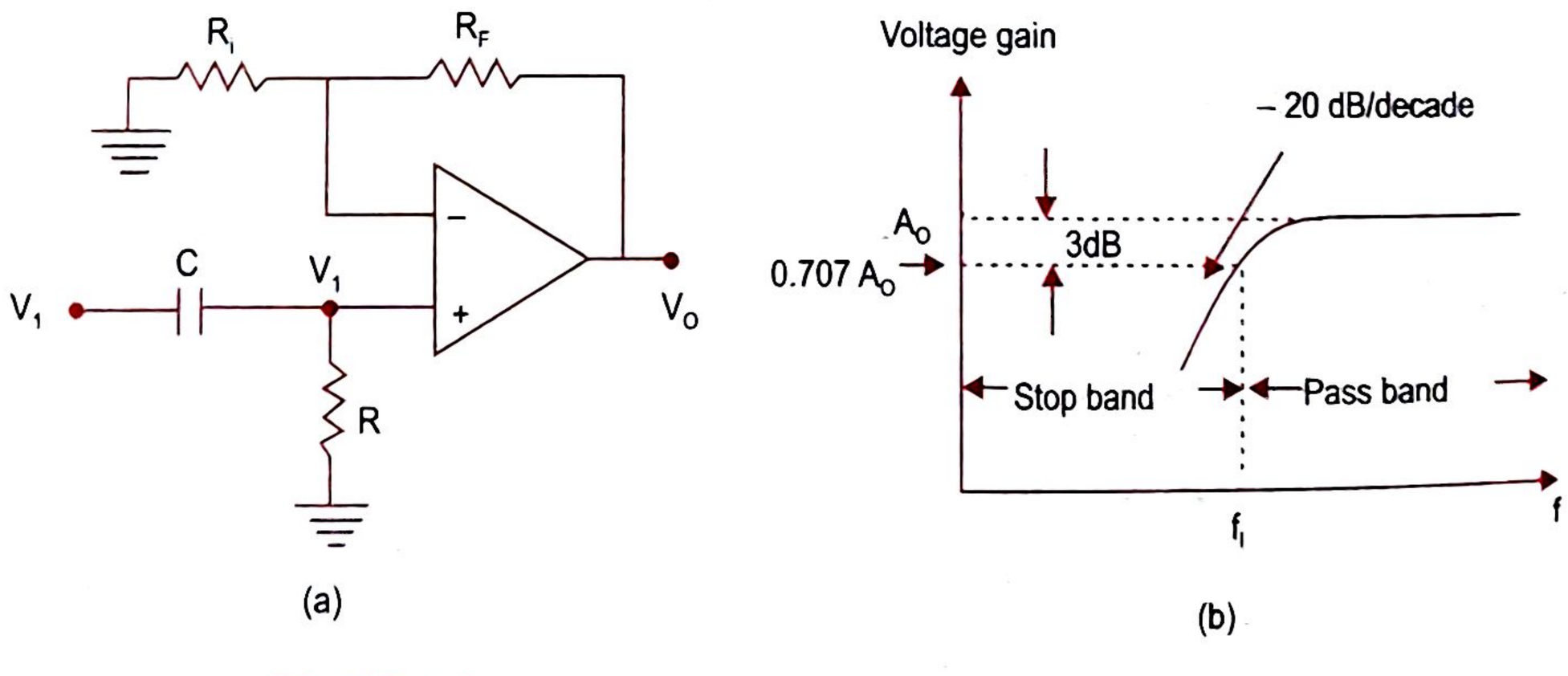


Fig 7.8 (a) First order high-pass filter. (b) Frequency response

The voltage V_1 at the non-inverting terminal is given by

$$V_1(s) = \frac{R}{R + \frac{1}{sC}} V_i(s) \tag{7.27}$$

or $$\frac{V_1(s)}{V_i(s)} = \frac{RCs}{1+RCs} \tag{7.28}$$

where $V(s)$ is the Laplace transform of v in time domain.

Further, output voltage V_o is given by

$$V_o(s) = \left(1 + \frac{R_F}{R_i}\right) V_i(s) \tag{7.29}$$

The closed loop gain of the op-amp is,

$$A_o = \frac{V_o(s)}{V_1(s)} = 1 + \frac{R_F}{R_C} \tag{7.30}$$

Thus, the overall transfer function is obtained as

$$H(S) = \frac{V_o(s)}{V_1(s)} = \frac{A_o \times RCs}{1 + RCs} \tag{7.31}$$

or

$$H_{HP}(j\omega) = \frac{A_o j f/f_l}{1 + j(f/f_l)} \quad [s = j\omega] \tag{7.32}$$

where,

$$f_l = \frac{1}{2\pi RC}$$

The frequency response of the filter is obtained from the magnitude, that is

$$|H_{HP}(jf)| = \left|\frac{V_o}{V_i}\right| = \frac{A_o f/f_l}{\sqrt{1 + (f/f_l)^2}} \tag{7.33}$$

$$= \frac{A_o}{\sqrt{1 + (f_l/f)^2}} \tag{7.34}$$

The frequency response of the first order high-pass filter is shown in Fig 7.8(b). At very high frequencies ie. $f > f_l$, the gain is constant at A_o, and for $f < f_l$, the gain rolls-off at a rate of –20 dB/decade. The frequency range below f_l is called the stop band and the frequency range above f_l is called the pass-band.

It may be noted that the high-pass filter can be obtained from the low pass filter by applying the transformation

$$\left.\frac{s}{\omega_o}\right|_{LP} = \left.\frac{\omega_o}{s}\right|_{HP} \tag{7.35}$$

Thus, a low pass filter can be converted to a high pass filter simply by interchanging R and C

Example 7.4

Design and plot the frequency response of a first order high pass filter for pass band gain of 2 and lower cut-off frequency of 2KHZ.

Solution

Given $f_l = 2$ kHz

Assume $C = 0.01\ \mu F$

since $$f_l = \frac{1}{2\pi RC}$$

Therefore, $$R = \frac{1}{2\pi f_l C}$$

$$= \frac{1}{2\pi \times 2 \times 10^3 \times 10^{-8}}$$

$$= 7.95 \text{ kHZ}$$

Further, to obtain pass band gain of 2,

$$A_v = 2 = 1 + \frac{R_F}{R_i}$$

Assume $R_F = R_i = 10\ k\Omega$

Thus, we can obtain pass band gain of 2. The frequency response data is shown in Table 7.3.

Table 7.3

Frequency (Hz)	*Gain* $\lvert V_o/V_i \rvert$	*Gain in dB* $20 \log \frac{V_o}{V_i}$
100	0.10	– 20.01
200	0.20	– 14.02
400	0.39	– 8.13
1000	0.89	– 0.97
3000	1.66	4.42
10,000	1.96	5.85
100 kHz	2.00	6.02

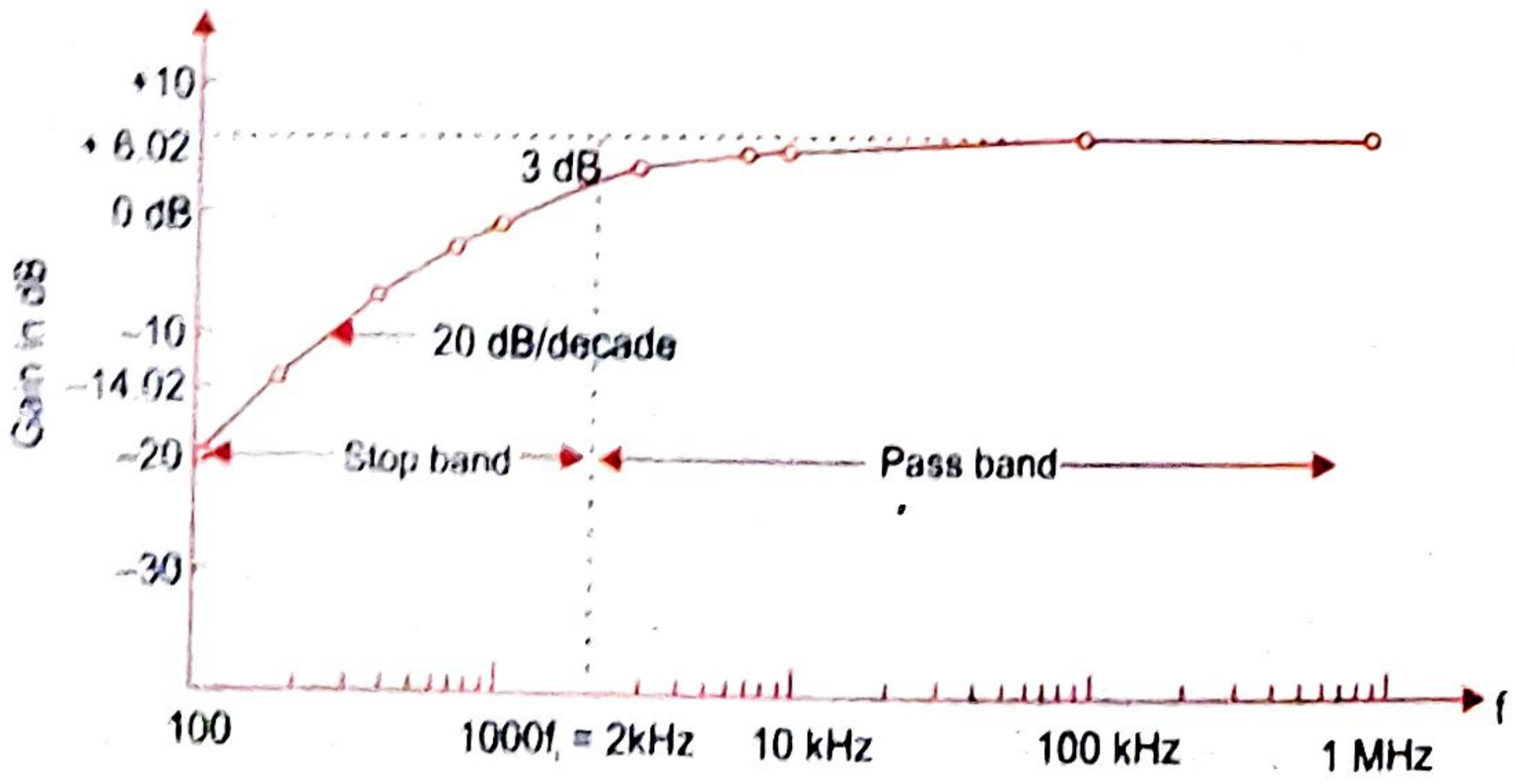


Fig. 7.9 Frequency response of first order high-pass filter.

Second Order High Pass Active Filter

High pass filter is the complement of the low pass filter and can be obtained simply by interchanging R and C in the low pass configuration and is shown in Fig. 7.10. Putting $Y_1 = Y_2 = sC$ and $Y_3 = Y_4 = G = 1/R$ in the general Eq. (7.17), the transfer function becomes.

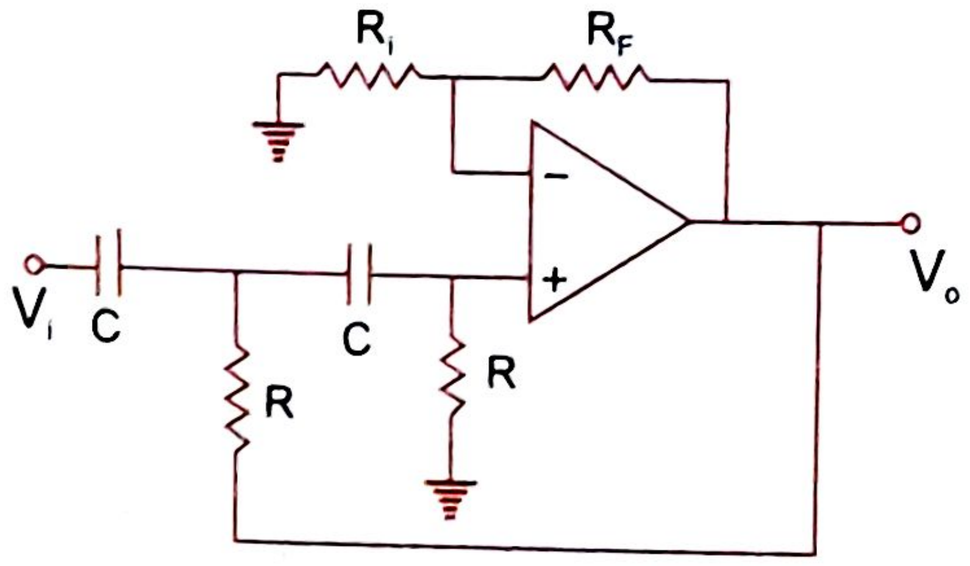


Fig. 7.10 Second order high pass filter

$$H_{HP}(s) = \frac{A_o s^2}{s^2 + (3 - A_o)\omega_l s + \omega_l^2} \qquad (7.36)$$

where $$\omega_l = \frac{1}{RC}$$

or, $$H_{HP}(s) = \frac{A_o}{1 + \frac{\omega_l}{s}(3 - A_o) + \left(\frac{\omega_l}{s}\right)^2} \qquad (7.37)$$

From Eq. (7.37), for $\omega = 0$, we get $H = 0$ and for $\omega = \infty$, we get $H_{HP} = A_o$. So the circuit indeed acts like high pass filter. The lower cut-off frequency

$$f_l = f_{3dB} = \frac{1}{2\pi RC}$$

and is same as in the low pass filter.

Putting $s = j\omega$ in Eq. (7.37) and $3 - A_o = \alpha = 1.414$, the voltage gain magnitude equation of the second order Butterworth high pass filter can be obtained as

$$|H_{HP}(j\omega)| = \left|\frac{V_o}{V_i}\right| = \frac{A_o}{\sqrt{1 + (f_l/f)^4}} \qquad (7.38)$$

Hence

$$\left|\frac{H_{HP}(j\omega)}{A_o}\right| = \frac{1}{\sqrt{1 + \left(\frac{f_l}{f}\right)^4}} \qquad (7.39)$$

Higher-order High-pass Filters

The magnitude of the voltage transfer function for the nth order Butterworth high-pass filter is given by

$$|H_{HP}(jf)| = \frac{1}{\sqrt{1 + \left(\frac{f_l}{f}\right)^{2n}}} \qquad (7.40)$$

Higher order filters can be designed by adding additional *RC* networks, that is by cascading a required number of first and second order filters. Fig 7.11 (a) and (b) shows a third-order and fourth order high pass Butterworth filter respectively.

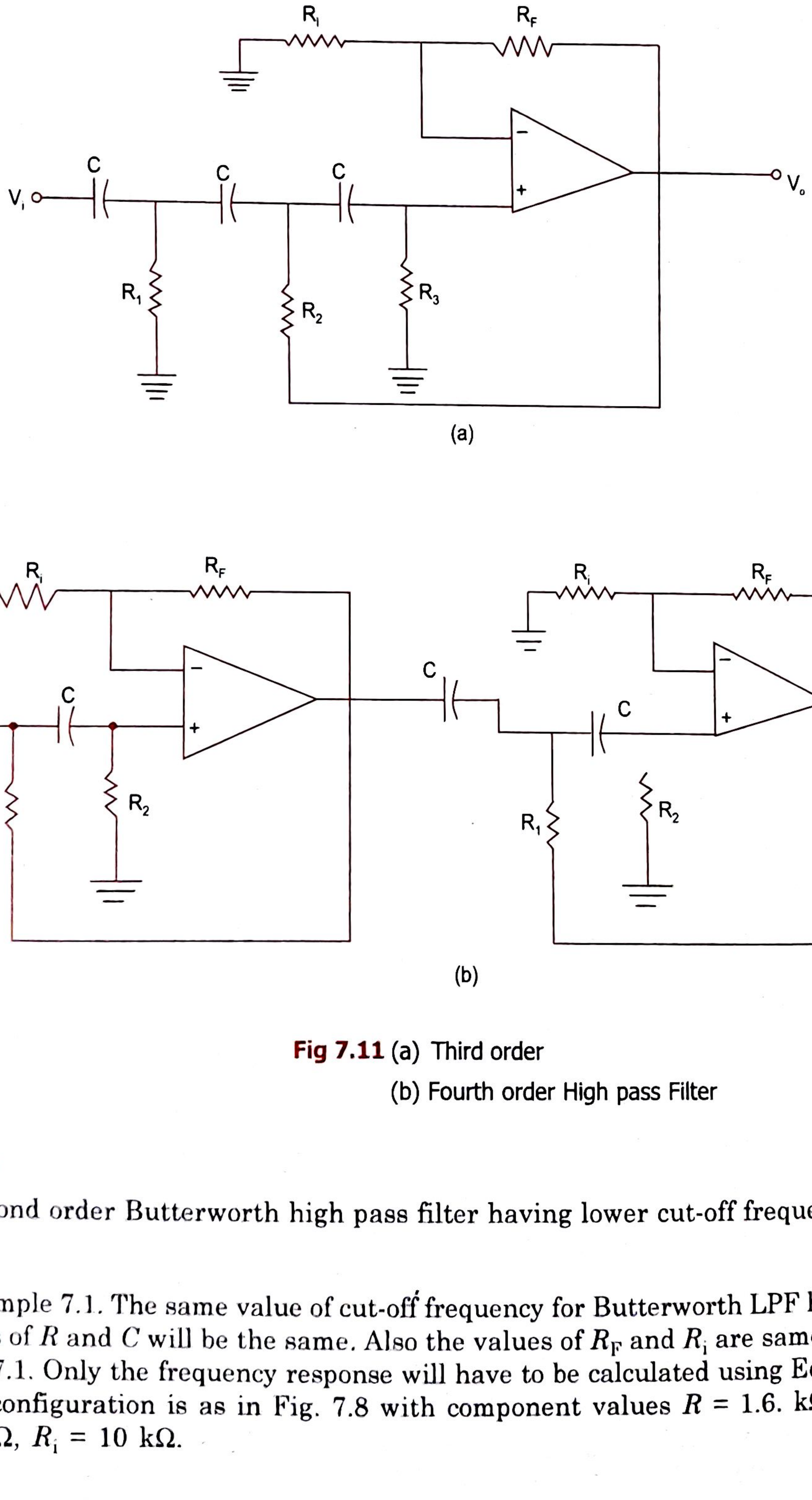


Fig 7.11 (a) Third order
(b) Fourth order High pass Filter

Example 7.5

Design a second order Butterworth high pass filter having lower cut-off frequency of 1 kHz.

Solution

Refer to Example 7.1. The same value of cut-off frequency for Butterworth LPF has been taken so the values of R and C will be the same. Also the values of R_F and R_i are same as calculated in Example 7.1. Only the frequency response will have to be calculated using Equation. (7.34). The circuit configuration is as in Fig. 7.8 with component values R = 1.6. kΩ, C = 0.1 μF, R_F = 5.86 kΩ, R_i = 10 kΩ.

7.25 Band Pass Filter

There are two types of band pass filters which are classified as per the figure of merit or quality factor Q.

(i) Narrow band pass filter ($Q > 10$)
(ii) Wide band pass filter ($Q < 10$)

The following relationships are important:

$$Q = f_o/BW = f_o/(f_h - f_l)$$

and

$$f_o = \sqrt{f_h f_l}$$

where f_h = upper cut-off frequency
f_l = lower cut-off frequency
f_o = the central frequency

Narrow Band Pass Filter

The important parameters in a band pass filter (BPF) are upper and lower cut-off frequencies (f_h and f_l), the band width (BW), the central frequency (f_o), the central frequency gain A_o and selectivity Q. Consider the circuit of Fig. 7.12 (a). The circuit has two feedback paths and the op-amp is used in inverting mode of operation.

The node voltage equation at node A is

$$v_i Y_1 + v_o Y_3 = v_A (Y_1 + Y_2 + Y_3 + Y_4) \tag{7.41}$$

Assuming, $v_B = 0$ (virtual ground), the node voltage equation at node B is,

$$v_A Y_2 = -v_o Y_5$$

$$v_A = -v_o (Y_5/Y_2) \tag{7.42}$$

Putting v_A in Eq. (7.41), we get

$$v_i Y_1 + v_o Y_3 = -\frac{v_o Y_5 (Y_1 + Y_2 + Y_3 + Y_4)}{Y_2}$$

or,

$$v_i Y_1 = v_o \left[-\frac{Y_2 Y_3 + Y_1 Y_5 + Y_2 Y_5 + Y_3 Y_5 + Y_4 Y_5}{Y_2} \right]$$

Hence

$$\frac{v_o}{v_i} = -\frac{Y_1 Y_2}{Y_2 Y_3 + Y_1 Y_5 + Y_2 Y_5 + Y_3 Y_5 + Y_4 Y_5} \tag{7.43}$$

For this circuit to be band pass filter, put $Y_1 = G_1$, $Y_2 = sC_2$, $Y_3 = sC_3$, $Y_4 = G_4$ and $Y_5 = G_5$ as shown in Fig. 7.12 (b). Then the transfer function becomes,

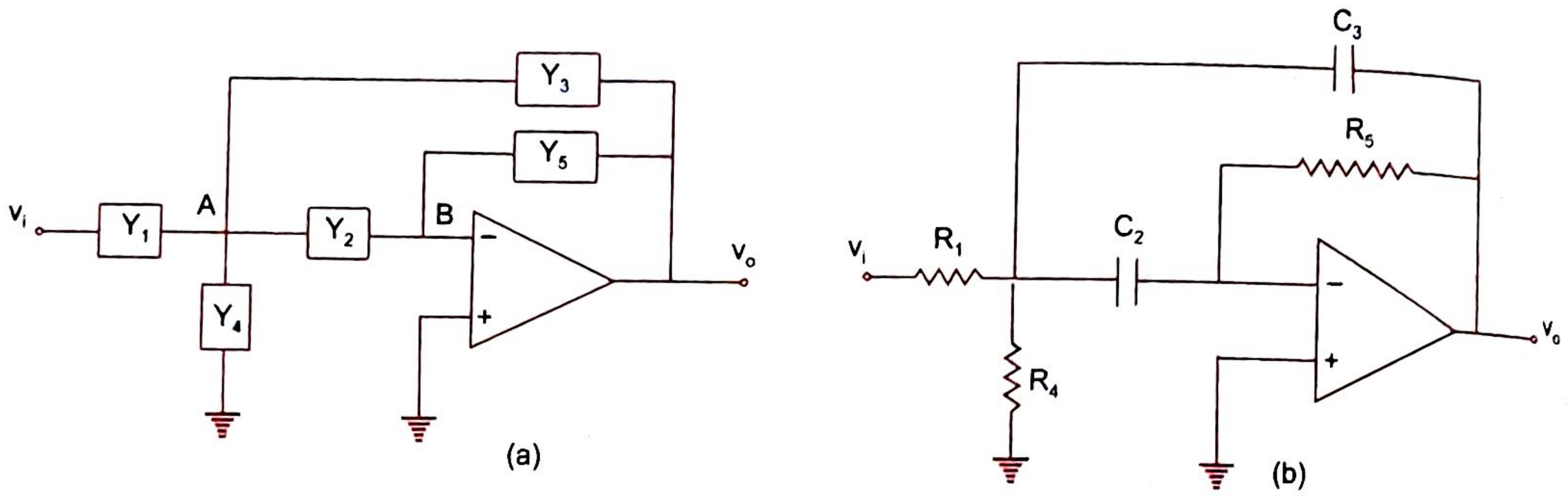


Fig. 7.12 (a) Band-pass configuration (b) Second order band-pass filter

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{-sG_1C_2}{s^2C_2C_3 + s(C_2 + C_3)G_5 + G_5(G_1 + G_4)}$$

or,
$$H(s) = \frac{-G_1}{sC_3 + G_5(C_2 + C_3)/C_2 + (G_1 + G_4)G_5/sC_2} \tag{7.44}$$

The transfer function of Eq. (7.44) is equivalent to the gain expression of a parallel RLC circuit of Fig. 7.13 (a) driven by a current source $G'v_i$ and with band pass characteristics as shown in Fig. 7.13 (b). The gain expression is,

$$\frac{V_o(s)}{V_i(s)} = -\frac{G'}{Y} = \frac{-G'}{sC + G + 1/sL} \tag{7.45}$$

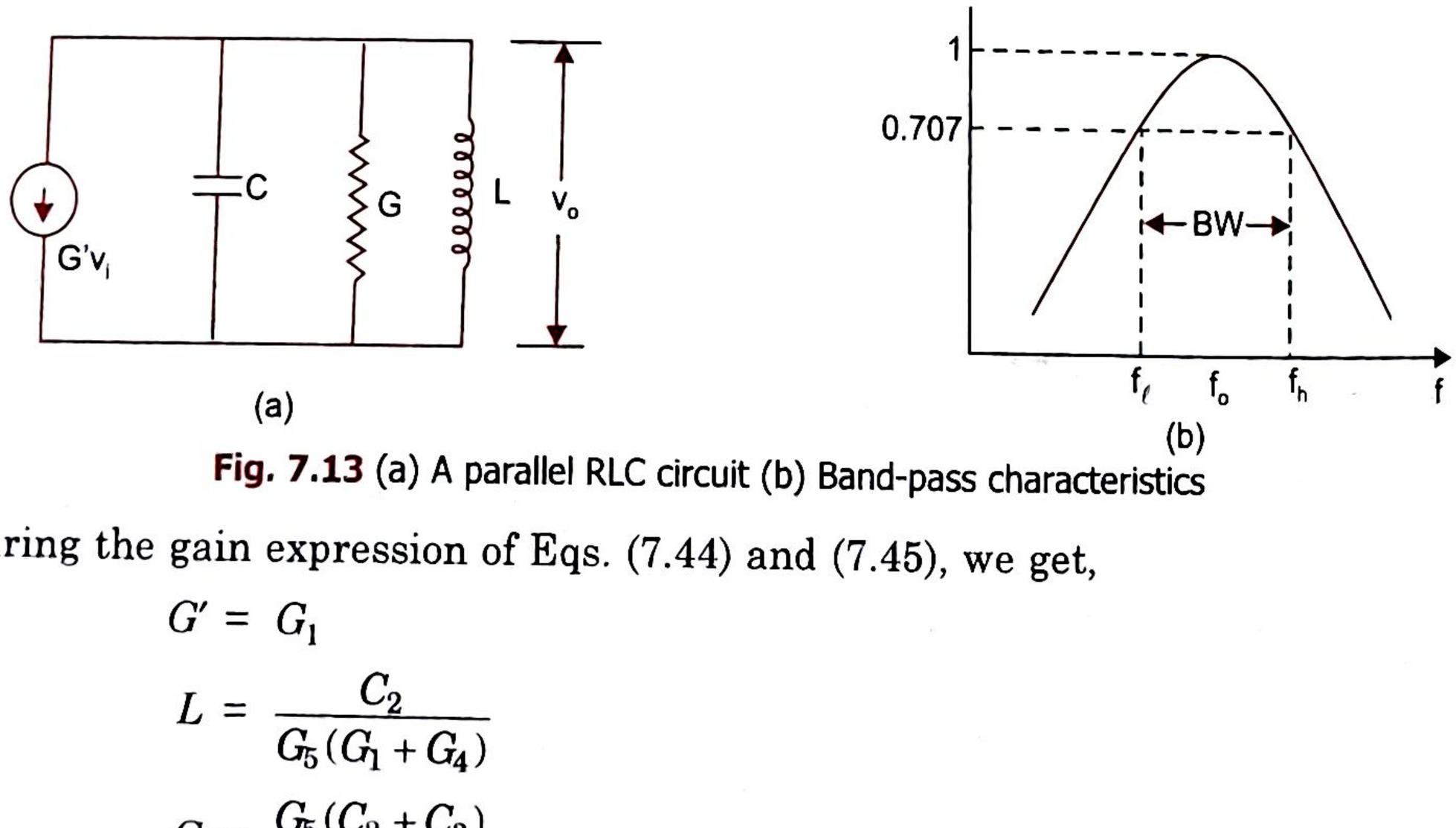


Fig. 7.13 (a) A parallel RLC circuit (b) Band-pass characteristics

Comparing the gain expression of Eqs. (7.44) and (7.45), we get,

$$G' = G_1 \tag{7.46}$$

$$L = \frac{C_2}{G_5(G_1 + G_4)} \tag{7.47}$$

$$G = \frac{G_5(C_2 + C_3)}{C_2} \tag{7.48}$$

and
$$C = C_3 \tag{7.49}$$

At resonance, the circuit of Fig. 7.13 (a) has unity power factor, i.e. imaginary part is zero which gives the resonant frequency ω_o as,

$$\omega_o^2 = \frac{1}{LC} = G_5\frac{(G_1 + G_4)}{C_2C_3} \tag{7.50}$$

The gain at resonance is,

$$\left.\frac{v_o}{v_i}\right|_{\omega=\omega_o} = -\frac{G'}{G} = -\frac{G_1}{G} = -\frac{(G_1/G_5)C_2}{C_2+C_3}$$

$$= -\frac{(R_5/R_1)C_2}{C_2+C_3} \tag{7.51}$$

The Q factor at resonance is,

$$Q_o = \frac{\omega_o L}{R} = \omega_o RC = \frac{\omega_o C}{G} = \frac{\omega_o C_2 C_3}{(C_2+C_3)G_5} \tag{7.52}$$

The bandwidth BW is given by,

$$BW = f_h - f_l = \frac{f_o}{Q_o} = \frac{\omega_o}{2\pi Q_o} = \frac{\omega_o}{2\pi R\omega_o C}$$

$$= \frac{1}{2\pi RC} = \frac{G}{2\pi C} = \frac{G_5(C_2+C_3)}{2\pi C_2 C_3} \tag{7.53}$$

and the centre frequency $f_o = \sqrt{f_h f_l}$

Now for $C_2 = C_3 = C$, the gain at resonant frequency from Eq. (7.51) is,

$$\left.\frac{v_o}{v_i}\right|_{\omega=\omega_o} = -\frac{R_5}{2R_1} = -A_o \tag{7.54}$$

$$\omega_o = \frac{\sqrt{G_5(G_1+G_4)}}{C} \tag{7.55}$$

$$BW = \frac{G_5}{\pi C} = \frac{1}{\pi R_5 C} \tag{7.56}$$

We have three independent design parameter Eqs. (7.54), (7.55) and (7.56) for gain at resonance, resonant frequency and bandwidth. But there are four unknown parameters of the circuit such as C, G_1, G_4 and G_5. So we have to choose any one parameter arbitrarily.

Figure 7.14 shows a plot of freq-uency response for different values of Q. The higher the Q, the sharper the filter. Below 0.5 f_o and above 2 f_o, all filters roll-off at – 20 dB/decade independent of the value of Q. This is limited by the two RC pairs in the circuit. To obtain sharper roll-off rate away from the center frequency, one should cascade several filters.

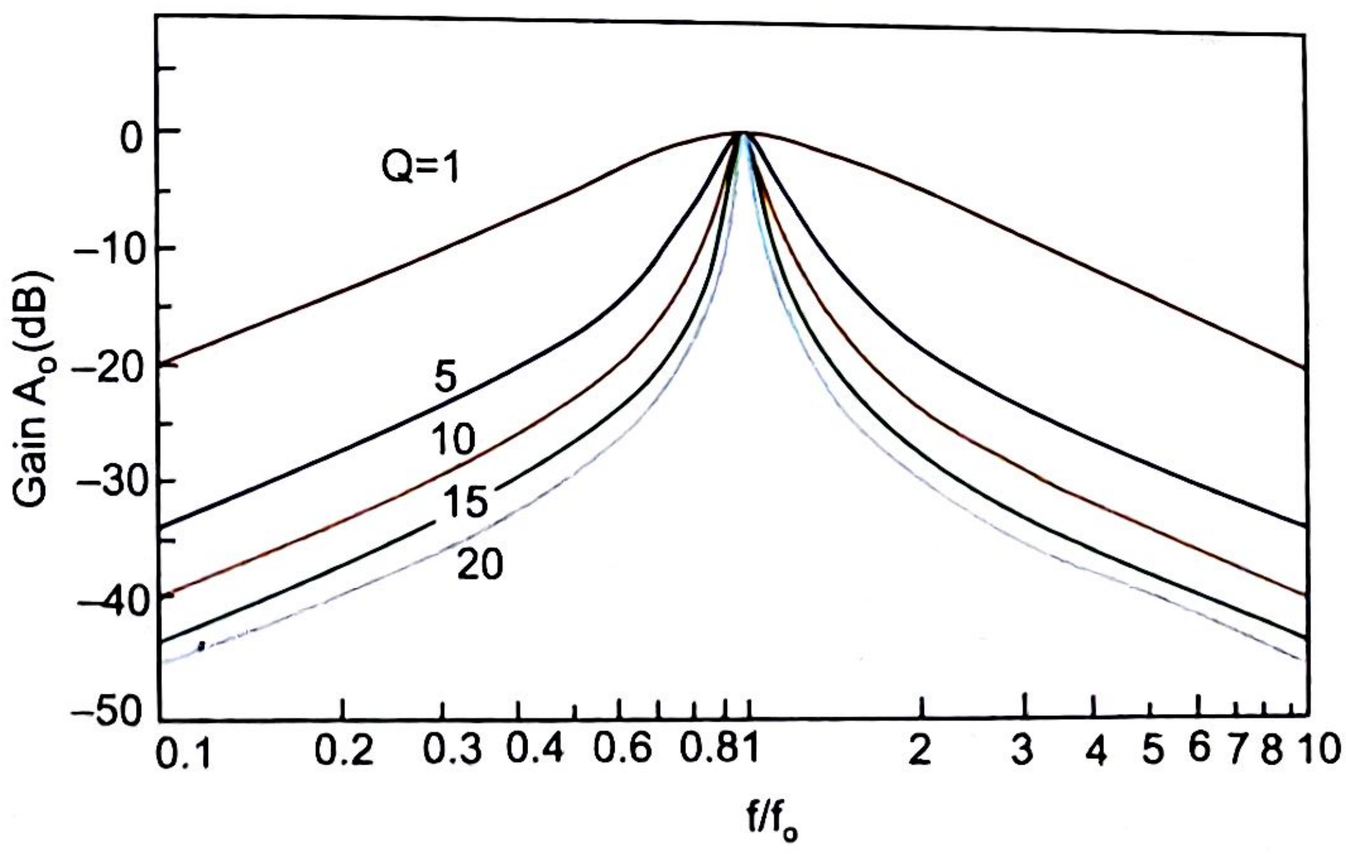


Fig. 7.14 Single op-amp band-pass filter response

It may further be noted that using Eqs. (7.52, 7.54 and 7.55) in Eq. (7.44), the standard transfer function of a bandpass filter is obtained as,

$$H(s) = \frac{-A_0(\omega_0/Q)s}{s^2 + (\omega_0/Q)s + \omega_0^2} = \frac{-A_0 \alpha \omega_0 s}{s^2 + \alpha\omega_0 s + \omega_0^2} \tag{7.57}$$

or, in dB, we get, $20 \log |H(s)| = 20 \log \left| \frac{A_0 \alpha \omega_0 s}{s^2 + \alpha \omega_0 s + \omega_0^2} \right|$ (7.58)

where the damping factor $\alpha = \frac{1}{Q}$.

It is obvious from Eq. (7.57) that for $\omega << \omega_0$ and $\omega >> \omega_0$, the gain is zero and for $\omega = \omega_0$ the gain is A_0. It may be noted that A_0 is negative.

Wide Band-Pass Filter

A wide band-pass filter can be formed by cascading a HPF and LPF section. If the HPF and LPF are of the first order, then the band-pass filter (BPF) will have a roll-off rate of – 20 dB/ decade.

For the high pass section of Fig. 7.15 the magnitude of gain is

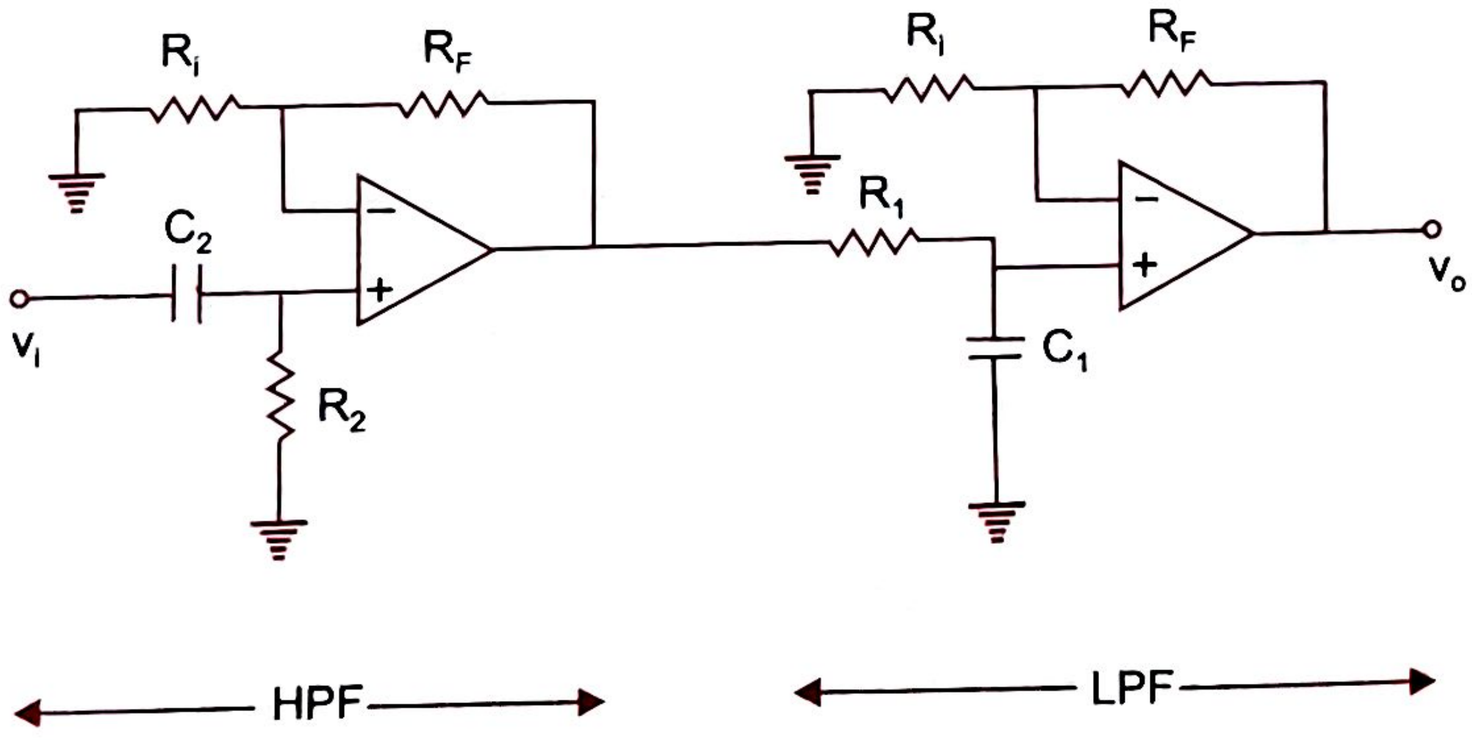


Fig. 7.15 First order band-pass filter

$$|H_{HP}| = \left| \left(1 + \frac{R_F}{R_i}\right) \frac{j\,2\pi f R_2 C_2}{1 + j2\pi f R_2 C_2} \right| = \left| A_{01} \frac{j(f/f_l)}{1 + j(f/f_l)} \right| = \frac{A_{01}(f/f_l)}{\sqrt{1 + (f/f_l)^2}} \tag{7.59}$$

where $f_l = \frac{1}{2\pi R_2 C_2}$ (7.60)

Similarly, for the low-pass section of Fig. 7.15, the magnitude of gain is

$$|H_{LP}| = \frac{A_{02}}{\sqrt{1 + (f/f_h)^2}} \tag{7.61}$$

where $f_h = \frac{1}{2\pi R_1 C_1}$ (7.62)

The voltage gain magnitude of the wide band pass filter is the product of that of LPF and HPF. One can calculate the frequency response from the equation

$$\left|\frac{v_o}{v_i}\right| = \left|\frac{A_o(f/f_l)}{\sqrt{\left[1+(f/f_l)^2\right]\left[1+(f/f_h)^2\right]}}\right| \tag{7.63}$$

where the total pass band gain $A_o = A_{o1} \times A_{o2}$.

In a similar fashion, to obtain BPF of –40 dB/decade fall-off rate, second order HPF and LPF sections are to be cascaded.

Example 7.6

Design a wide-band pass filter having $f_l = 400$ Hz, $f_h = 2$ kHz and pass band gain of 4. Find the value of Q of the filter.

Solution

The pass band gain is 4. The LPF and HPF sections each of Fig. 7.15 may be designed to give gain of 2, that is, $A_o = 1 + R_F/R_i = 2$. So R_F and R_i should be equal. Let $R_F = R_i = 10$ kΩ for each of LPF and HPF sections.

For LPF, $f_h = 2$ kHz $= 1/2\,\pi\, R_1C_1$. Let $C_1 = 0.01$ μF gives $R_1 = 7.9$ kΩ. For HPF, $f_l = 400$ Hz $= 1/2\,\pi\, R_2C_2$. Let $C_2 = 0.01$ μF gives $R_2 = 39.8$ kΩ.

Again $f_o = \sqrt{f_h f_l} = \sqrt{2000 \times 400} = 894.4$

$$Q = f_o/BW = f_o/(f_h - f_l) = 894.4/(2000 - 400) = 0.56$$

Obviously, for wide band pass filter, Q is very low, i.e., $Q < 10$.

Example 7.7

The resonant frequency f_o of a band-pass filter is 1 kHz and its BW is 3 kHz. Find (i) Q (ii) f_l and f_h.

Solution

We know that quality factor, Q is given by,

(i) $$Q = \frac{f_o}{BW} = \frac{1\times10^3}{3\times10^3} = 0.33$$

Since $Q < 10$, it is a wide band filter.

(ii) It can be shown that

$$f_l = \sqrt{\frac{BW^2}{4} + f_o^2} - \frac{B}{2}$$

and $f_h = f_l + BW,$

we find $f_l = 302.77$ Hz

and $f_h = 3302.77$ Hz

7.2.6 Band Reject Filter

A band reject filter (also called a band stop or band elimination) can be either (i) Narrow band reject filter or (ii) Wide band reject filter. The narrow band reject filter is commonly called a ***notch filter*** and is useful for the rejection of a single frequency, such as 50 Hz power line frequency hum.

There are several ways to make notch filters. One simple technique is to subtract the band pass filter output from its input. This principle is illustrated in Fig. 7.13 (a).

The band pass filter discussed earlier has an inverted output as the gain or transfer Eq. (7.35) is negative. Therefore, while implementing Fig. 7.13 (a), we must use a summer instead of a subtractor. Also, the band pass filter has a gain of A_o, so that output at the centre frequency will be $-A_o \times v_i$. To completely subtract this output, the input of the summer must be precisely $A_o v_i$. Thus, a gain of A_o must be added between the input signal and the summer as shown in Fig. 7.13 (b). The output, of the circuit in the s domain is,

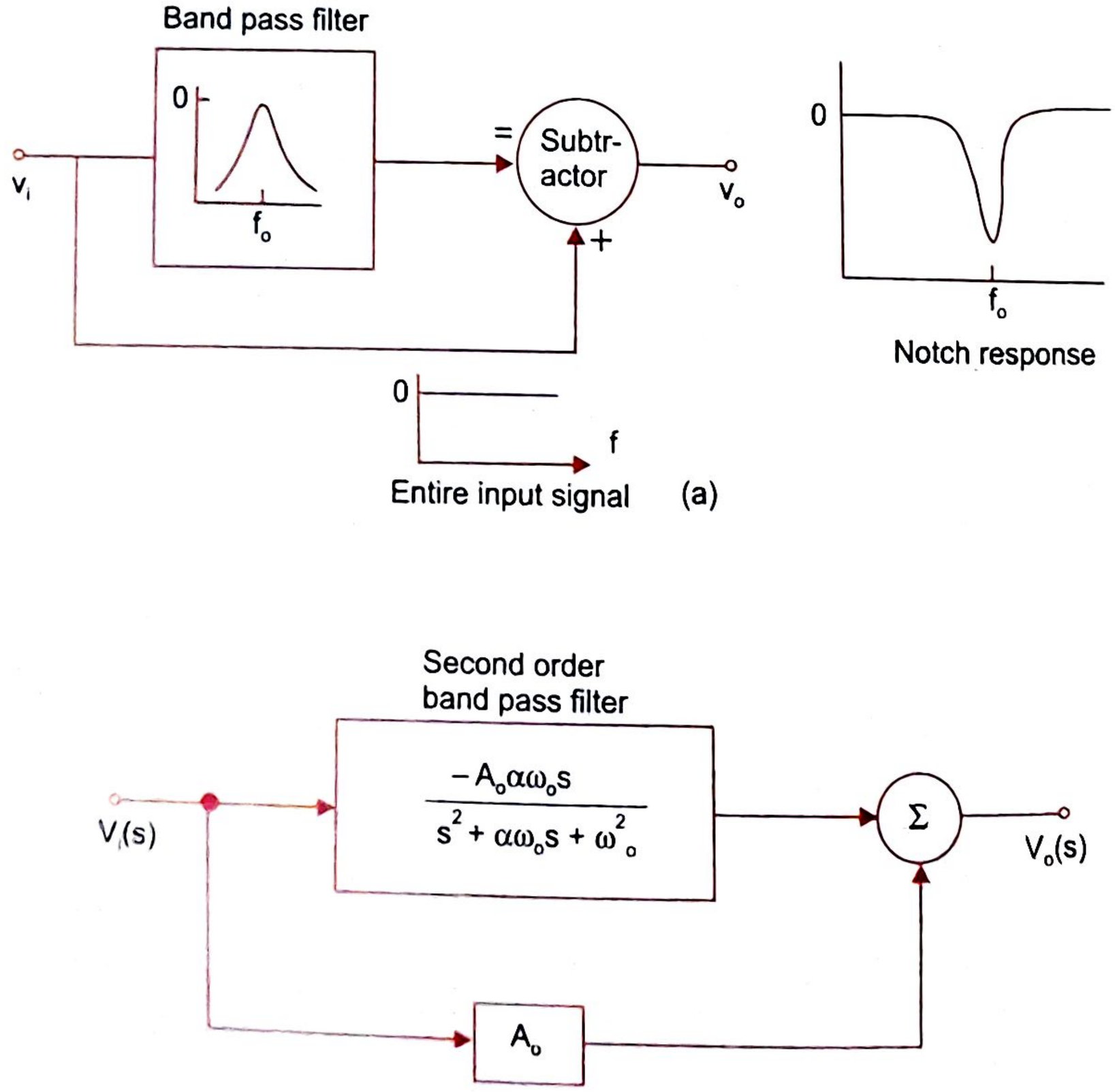


Fig. 7.16 (a) Notch filter block diagram (b) Practical notch filter block diagram

$$V_o(s) = A_o V_i(s) + \left(\frac{-A_o \alpha \omega_o s V_i(s)}{s^2 + \alpha \omega_o s + \omega_o^2} \right) \tag{7.64}$$

$$\frac{V_o(s)}{V_i(s)} = A_o - \frac{A_o \alpha \omega_o s}{s^2 + \alpha \omega_o s + \omega_o^2}$$

$$= A_o \left(1 - \frac{\alpha \omega_o s}{s^2 + \alpha \omega_o s + \omega_o^2} \right)$$

$$= \frac{A_o (s^2 + \omega_o^2)}{s^2 + \alpha \omega_o s + \omega_o^2} \tag{7.65}$$

This is the transfer function for a second order notch filter and the circuit schematic is shown in Fig. 7.17. It is evident from Eq. (7.65), that for $\omega << \omega_o$ and for $\omega >> \omega_o$ the pass band gain is $|A_o|$ and at frequency $\omega = \omega_o$ the gain is zero.

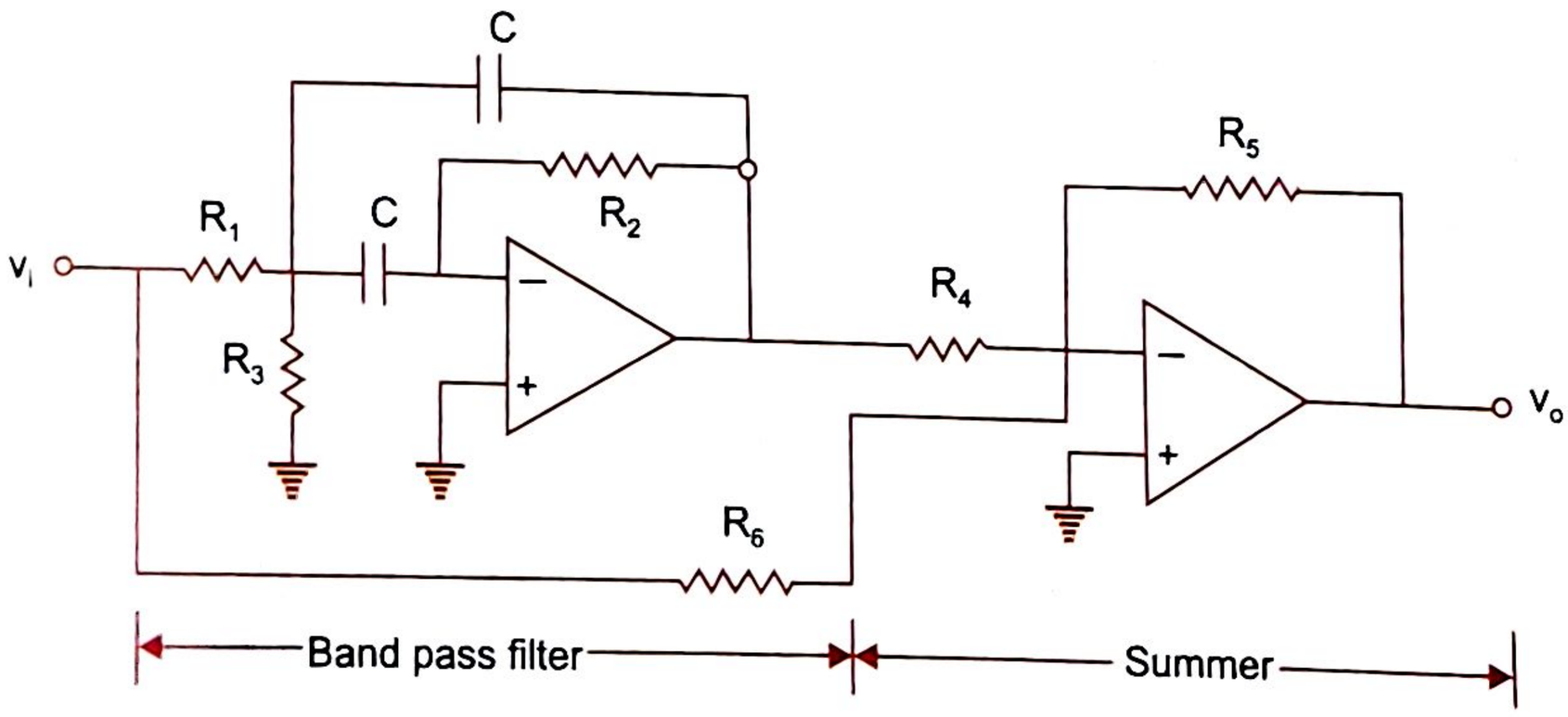


Fig. 7.17 Notch filter schematic

Another commonly used notch filter is the twin-T network as shown in Fig. 7.18 (a). We will determine the notch frequency, Q factor and bandwidth for this configuration.

Node voltage equations in s-domain (by KCL) for the active filter circuit of Fig. 7.18 (a) can be written as,

At node A: $(V_i - V_A)\, sC + (V_o - V_A)\, sC + (KV_o - V_A)2G = 0$

or, $$sC\, V_i + (sC + 2KG)\, V_o = 2\,(sC + G)\, V_A \tag{7.66}$$

where V_A is the Laplace transform of the voltage at node A. Similarly V_i and V_o are transformed input and output. The s in the parenthesis has been dropped in the Laplace transform for simplicity.

At node B: $(V_i - V_B)G + (V_o - V_B)G + 2\,(KV_o - V_B)sC = 0$

or, $$GV_i + (G + 2\,KsC)\, V_o = 2(G + sC)V_B \tag{7.67}$$

where V_B is the Laplace transform of the voltage at node B.

At node P: $(V_A - V_o)\, sC + (V_B - V_o)G = 0$

or, $$sC\, V_A + GV_B = (G + sC)V_o \tag{7.68}$$

where, $K = R_2/(R_1 + R_2)$ and $G = 1/R$

From these node voltage equations, the transfer function can be written as,

$$H(s) = \frac{V_o}{V_i} = \frac{G^2 + s^2C^2}{G^2 + s^2C^2 + 4(1-K)sCG}$$

$$= \frac{s^2 + (G/C)^2}{s^2 + (G/C)^2 + 4(1-K)s(G/C)} \quad (7.69)$$

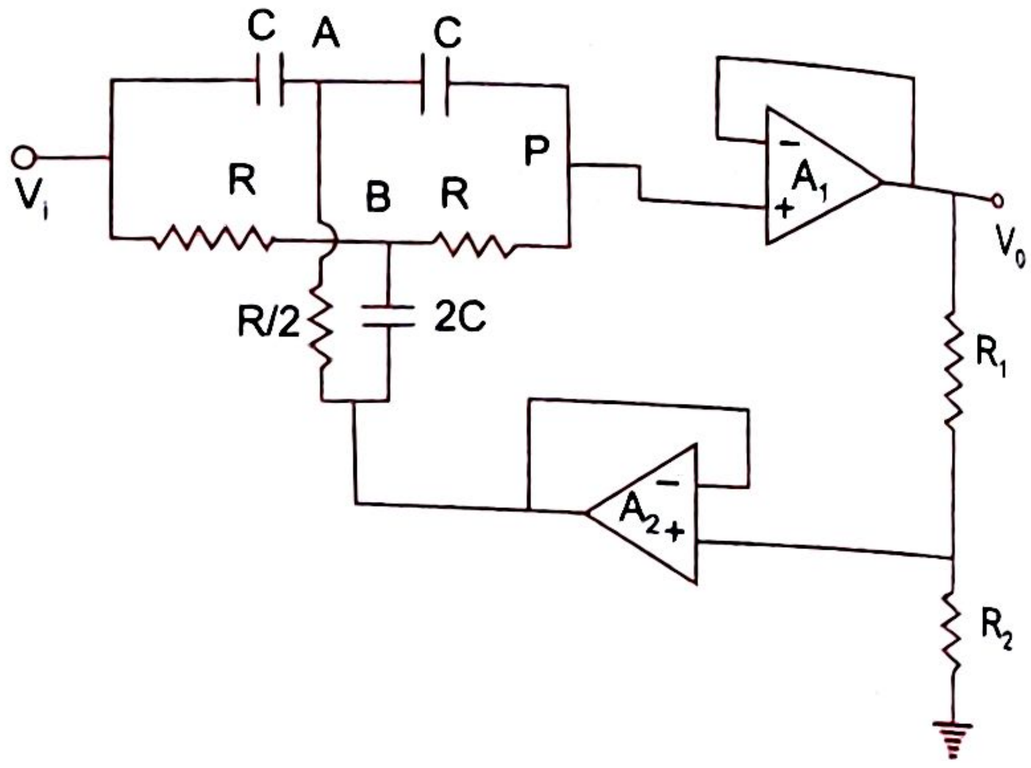


Fig. 7.18 (a) Twin-T notch filter

In the steady state (i.e. $s = j\omega$),

$$H(j\omega) = \frac{\omega^2 - \omega_o^2}{\omega^2 - \omega_o^2 - j4(1-K)\omega\omega_o} \quad (7.70)$$

where, $\omega_o = G/C = 1/RC$

i.e., $$f_o = \frac{1}{2\pi RC} \quad (7.71)$$

From Eq. (7.70), $H(j\omega)$ becomes zero for $\omega = \omega_o$ and approaches unity as $\omega << \omega_o$ and for $\omega >> \omega_o$. In practice, the high frequency response will be limited by the high frequency response of the op-amp. At 3-dB points, $|H| = 1/\sqrt{2}$

i.e. $$\omega^2 - \omega_o^2 = \pm 4(1-K)\,\omega\,\omega_o$$

or $$(\omega/\omega_o)^2 \pm 4(1-K)\,(\omega/\omega_o) - 1 = 0 \quad (7.72)$$

Solving the quadratic equation, we get the upper and lower half power frequencies as,

$$f_h = f_o\left[\sqrt{1 + 4(1-K)^2} + 2(1-K)\right] \quad (7.73)$$

and $$f_l = f_o\left[\sqrt{1 + 4(1-K)^2} - 2(1-K)\right] \quad (7.74)$$

The 3-dB bandwidth,

$$BW = f_h - f_l = 4(1-K)f_o \quad (7.75)$$

$$Q = \frac{f_o}{BW} = \frac{1}{4(1-K)} \quad (7.76)$$

As K approaches unity, Q factor becomes very large and BW approaches 0. In fact, mismatches between resistors and capacitors limit the Q-factor and BW to practically realizable value. It is advisable to use the components of 0.1 per cent tolerance resistors and 1 per cent tole-rance capacitors for very high value of Q-factor. The frequency response is shown in Fig. 7.18 (b).

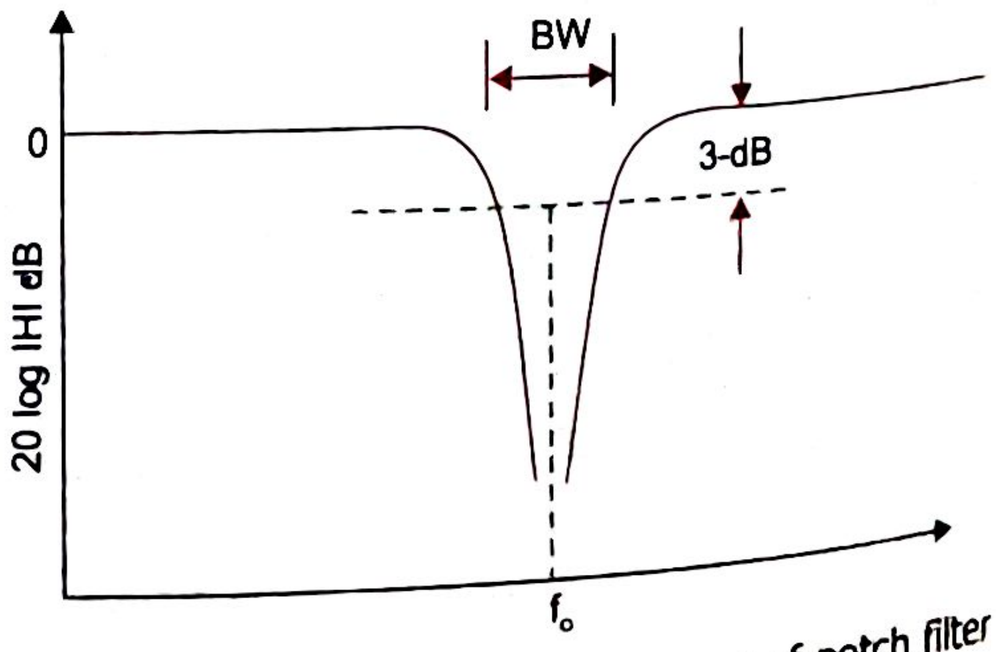


Fig. 7.18 (b) Frequency response of notch filter

Example 7.8

Design a 50 Hz active notch filter.

Solution

Given $f_o = 50$ Hz. Let $C = 0.1$ μF then from Eq. (7.62), we get $R = 1/2\,\pi f_o C = 1/2$ (3.14) (50) $(10^{-7}) = 31.8$ kΩ.

For $R/2$, take two resistors of 31.8 kΩ in parallel and for $2C$, take two 0.1 μF capacitors in parallel to make the twin-T notch filter as shown in Fig. 7.15 (a) where resistors R_1 and R_2 are for adjustment of gain.

Wide Band-Reject Filter

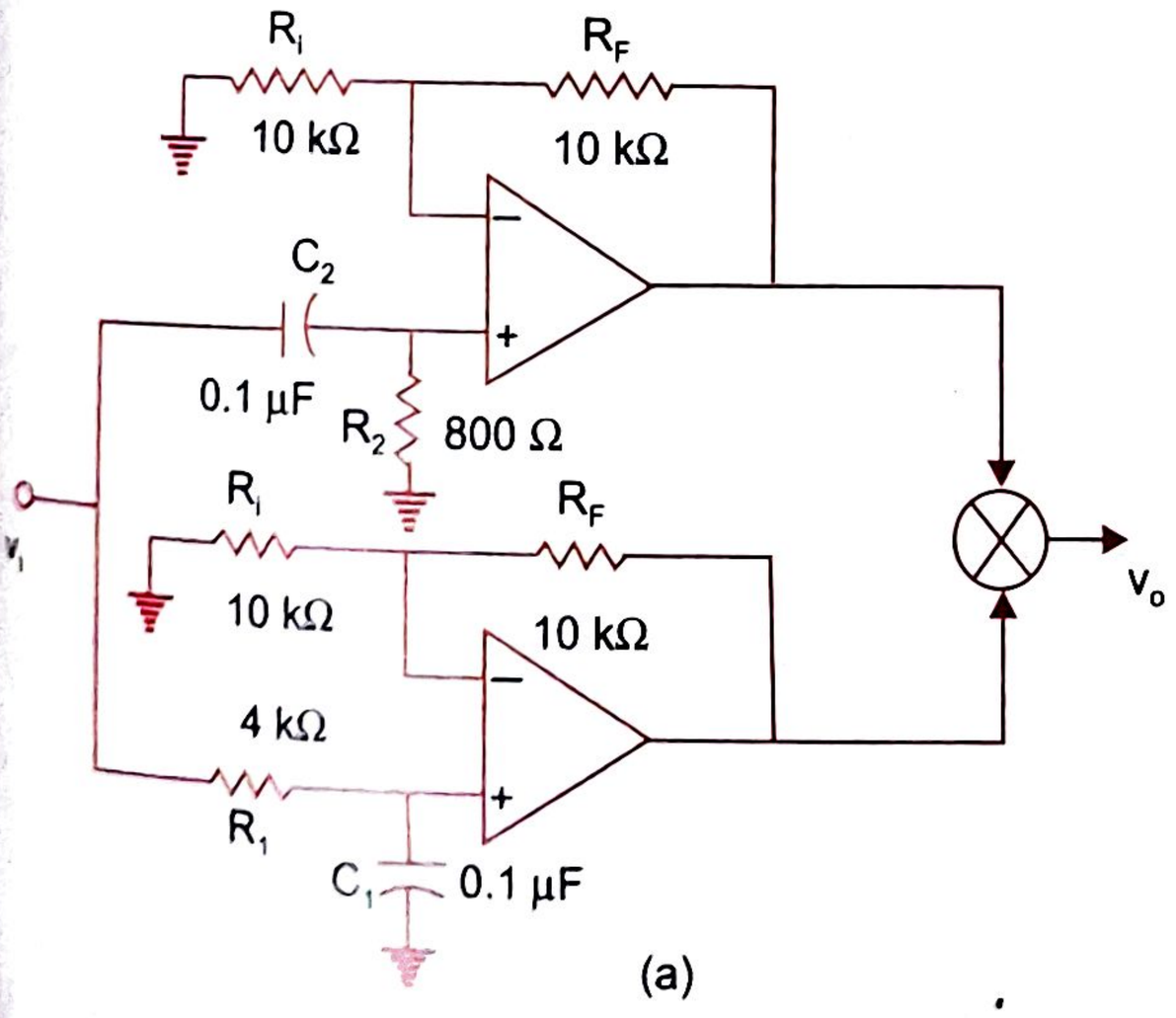
A wide band-reject filter ($Q < 10$) can be made using a LPF, HPF and a summer. It is of course necessary that (i) the lower cut off-frequency f_l of the HPF should be much greater than the upper cut-off frequency f_h of the LPF and (ii) the pass band gain of LPF and HPF should be same.

Example 7.9

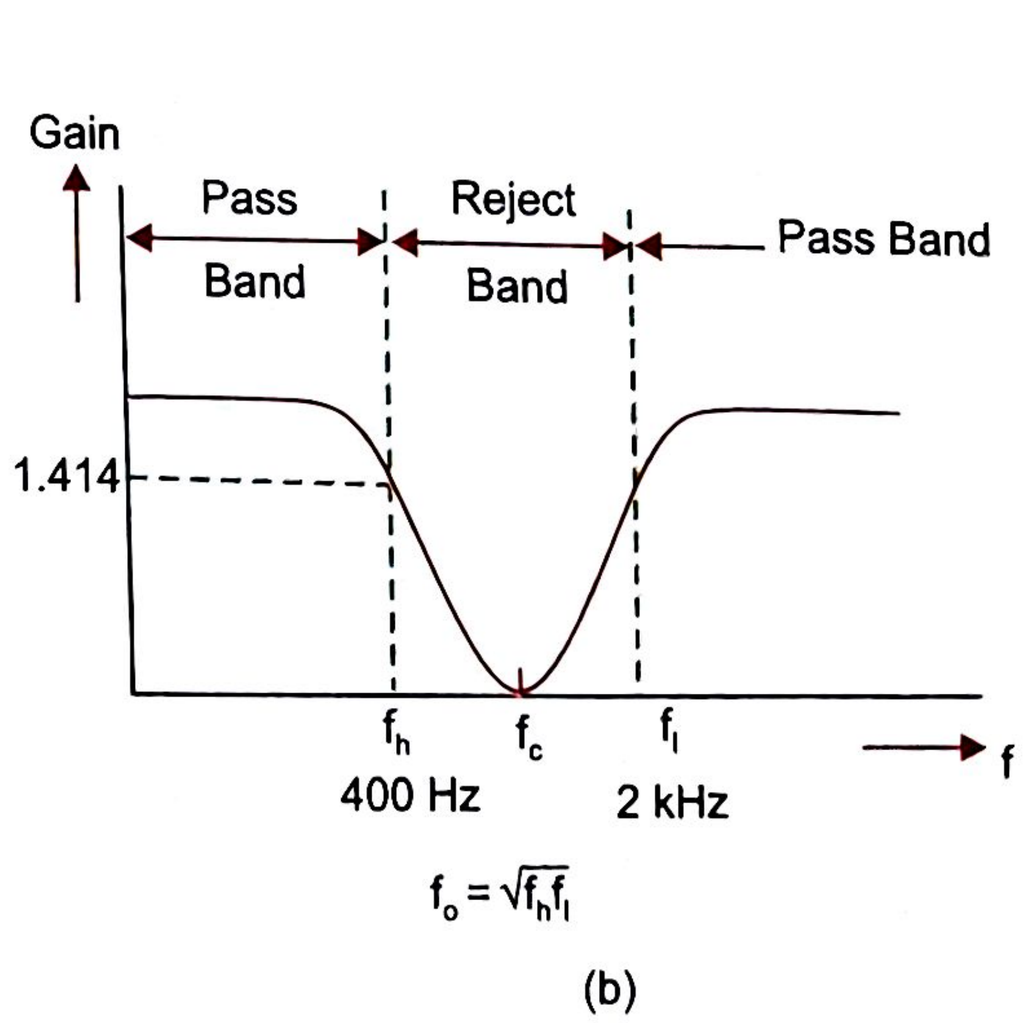
Design a wide band reject filter having $f_h = 400$ Hz and $f_l = 2$ kHz having pass band gain as 2.

Solution

For HPF, $f_l = 2$ kHz $= 1/2\,\pi R_2 C_2$. Letting $C_2 = 0.1$ μF gives $R_2 = 795\,\Omega$ ($\approx 800\,\Omega$). Again $A_o = A_{o2} = 2 = (1 + R_F/R_i)$ gives $R_F = R_i = 10$ kΩ (say). For LPF, $f_h = 400$ Hz $= 1/2\,\pi R_1 C_1$. Letting $C_1 = 0.1$ μF gives $R_1 = 3978\,\Omega$ (choose 4 kΩ). Further $A_o = A_{o1} = 2 = (1 + R_F/R_i)$ gives $R_i = R_F = 10$ kΩ (say). The schematic arrangement and the frequency response is shown in Figs. 7.16 (a, b).



(a)



(b)

Fig. 7.19 (a) Wide band-reject filter (b) Frequency response

7.2.7 All Pass Filter

An all-pass filter passes all frequency components of the input signal without any attenuation and provides desired phase shifts at different frequencies of the input signal. When singals are transmitted over transmission lines, such as telephone wires, they undergo change in phase. These phase changes can be compensated by all-pass filters. Thus, all pass filters are

also called delay equalizers or phase correctors. Figure 7.20 (a) shows an all-pass filter where $R_F = R_1$. The output voltage, v_o is obtained by using the superposition theorem:

$$v_o = \frac{-R_F}{R_1} v_i + \left(1 + \frac{R_F}{R_1}\right) v_a \tag{7.77}$$

where v_a is the voltage at node 'A'.

Since $R_F = R_1$, Eq. (7.77) may be written as

$$v_o = -v_i + 2v_a \tag{7.78}$$

where, $$v_a = \frac{-jX_C}{R - jX_C} \times v_i \tag{7.79}$$

Putting the value of 'v_a' from Eq. (7.79) to Eq. (7.78), we get,

$$v_o = -v_i + 2.\frac{-jX_C}{R - jX_C} v_i \tag{7.80}$$

$$= v_i \left(-1 - \frac{2}{1 + j2\pi f RC}\right) \tag{7.81}$$

or $$\frac{v_o}{v_i} = \left(\frac{1 - j2\pi f RC}{1 + j2\pi f RC}\right) \tag{7.82}$$

The magnitude of $\frac{v_o}{v_i}$ is given by

$$\frac{|v_o|}{|v_i|} = \frac{\sqrt{1 + (2\pi fRC)^2}}{\sqrt{1 + (2\pi fRC)^2}} \tag{7.83}$$

It can be seen that $|v_o| = |v_i|$ throughout the frequency range. The phase shift ϕ between v_o and v_i is given by

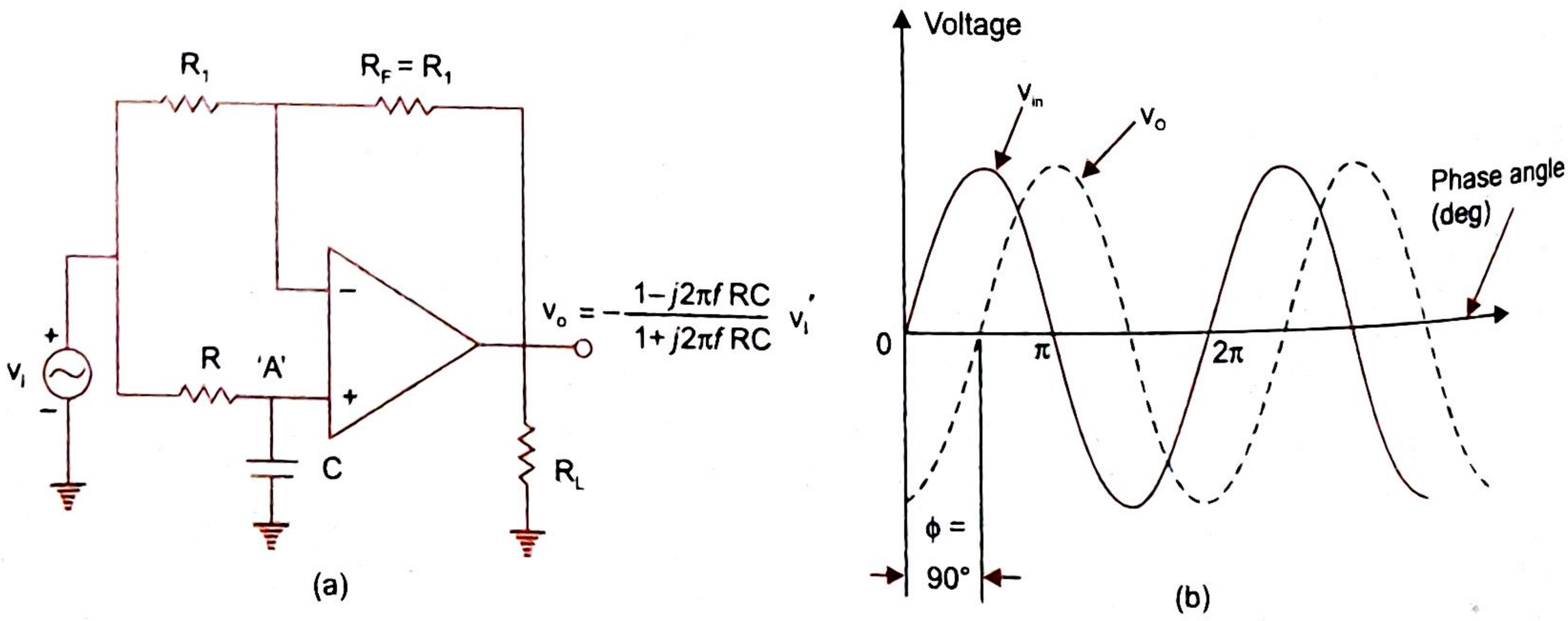


Fig. 7.20 (a) An all-pass filter (b) Input-output waveform for $\phi = 90°$

$$\phi = -\tan^{-1} 2\pi f RC - \tan^{-1} 2\pi f RC \qquad (7.84\ (a))$$

$$= -2 \tan^{-1}(2\pi f RC) \qquad (7.84\ (b))$$

Thus, the phase shift ϕ can be varied with frequency for a given R and C, and can be varied from 0 to –180° as the frequency is varied from 0 to ∞. As phase shift obtained is negative, the output v_o lags v_{in}. The phase shift can be made positive by interchanging R and C in Fig 7.20 (a).

If $R_F = R_1 = 10$ kΩ; $R = 15.9$ kΩ and $C = 0.01$ μF, using Eq. (7.75(b)), it can be seen that $\phi = -90°$. The output voltage v_o will have the same frequency as the input, but lags v_i by 90° as shown in Fig. 7.20 (b).

7.3 TRANSFORMATION

We shall now show that a high-pass, band-pass or band-reject filter can be obtained using an ideal low-pass transfer function by simple frequency transformation. For simplicity, let us normalize the frequency such that the cut-off frequency of the low pass function is unity. Let 'p' be the frequency domain of the low pass and 's' the frequency domain of interest.

Low Pass to High Pass Transformation

We get the high-pass characteristics by the following low-pass to high-pass transformation $p = 1/s$. For example, a third order Butterworth low-pass transfer function in p-domain given as

$$H(p) = \frac{A_0}{p^3 + 2p^2 + 2p + 1} \qquad (7.85)$$

can be transformed to high-pass by the transformation $p = 1/s$ as

$$H(s) = \frac{A_0 s^3}{s^3 + 2s^2 + 2s + 1} \qquad (7.86)$$

The high-pass filter has the same pass band flatness as that of the Butterworth low-pass filter.

A low-pass filter can be transformed to a high-pass filter simply by interchanging R and C components and vice versa. A simple $RC : CR$ transformation is shown in Fig. 7.4 and Fig. 7.10. This is to note that the 3-dB (cut-off) frequency is the same for both the original low-pass and the transformed high-pass filter i.e., $f_{3\text{–dB}} = 1/2\ \pi\ RC$.

Low Pass to Band Pass Transformation

Consider a first order Butterworth low-pass transfer function in p-domain as

$$H(p) = \frac{A_0}{p + 1} \qquad (7.87)$$

Let the transformation

$$p = \frac{s^2 + \omega_0^2}{(\omega_h - \omega_l)s} \qquad (7.88)$$

In order to normalize, put

$$s_n = s/\omega_o \tag{7.89}$$

and quality factor, $$Q = \frac{\omega_o}{\omega_h - \omega_l}$$

Then Eq. (7.88) can be rewritten as

$$p = \frac{Q(s_n^2 + 1)}{s_n} \tag{7.90}$$

Substituting the transformation from Eq. (7.90) to Eq. (7.87), we get

$$H(s_n) = \frac{(A_o/Q)s_n}{s_n^2 + (1/Q)s_n + 1} \tag{7.91}$$

This is identical with Eq. (7.57) of band pass filter. The quality factor Q is an important parameter. If Q is very high, i.e. $Q >> 1$, the filter is called narrow band filter (i.e., $\omega_o >> (\omega_h - \omega_l)$) and the response is symmetric about the central frequency ω_o.

Low Pass to Band Reject Transformation

The transformation is given by

$$p = \frac{(\omega_h - \omega_l)s}{s^2 + \omega_o^2} = \frac{s_n}{Q(s_n^2 + 1)} \tag{7.92}$$

where $s_n = s/\omega_o$

The band-reject transfer function corresponding to first order low-pass of Eq. (7.70) and is given by

$$H(s_n) = \frac{A_o(s_n^2 + 1)}{s_n^2 + (1/Q)s_n + 1} \tag{7.93}$$

Note at $s_n = j1$, $|H(j1)| = 0$. Such filters are called 'notch filter' with normalized null frequency as $\omega_o = 1$.

7.4 STATE VARIABLE FILTER

The state variable configuration uses two op-amp integrators and one op-amp adder to provide simultaneous second order low-pass, band-pass and high-pass filter responses. The circuit can be viewed as analog computer simulation of biquadratic transfer function. Although, in general, all component values are different, imposing equal value simplifies algebra without diminishing versatility.

A simple state variable configuration has been shown in Fig. 7.21 (a). It uses two op-amp integrators and one op-amp summer. The outputs v_{HP}, v_{BP}, v_{LP} of high-pass, band-pass and low-pass filters are obtained at the output of op-amp A_1, A_2 and A_3 respectively. For simplification, it is assumed that V is the Laplace transform of the corresponding v in time domain.

The op-amp A_2 works as an inverting integrator, so the Laplace transformed output V_{BP} is given by

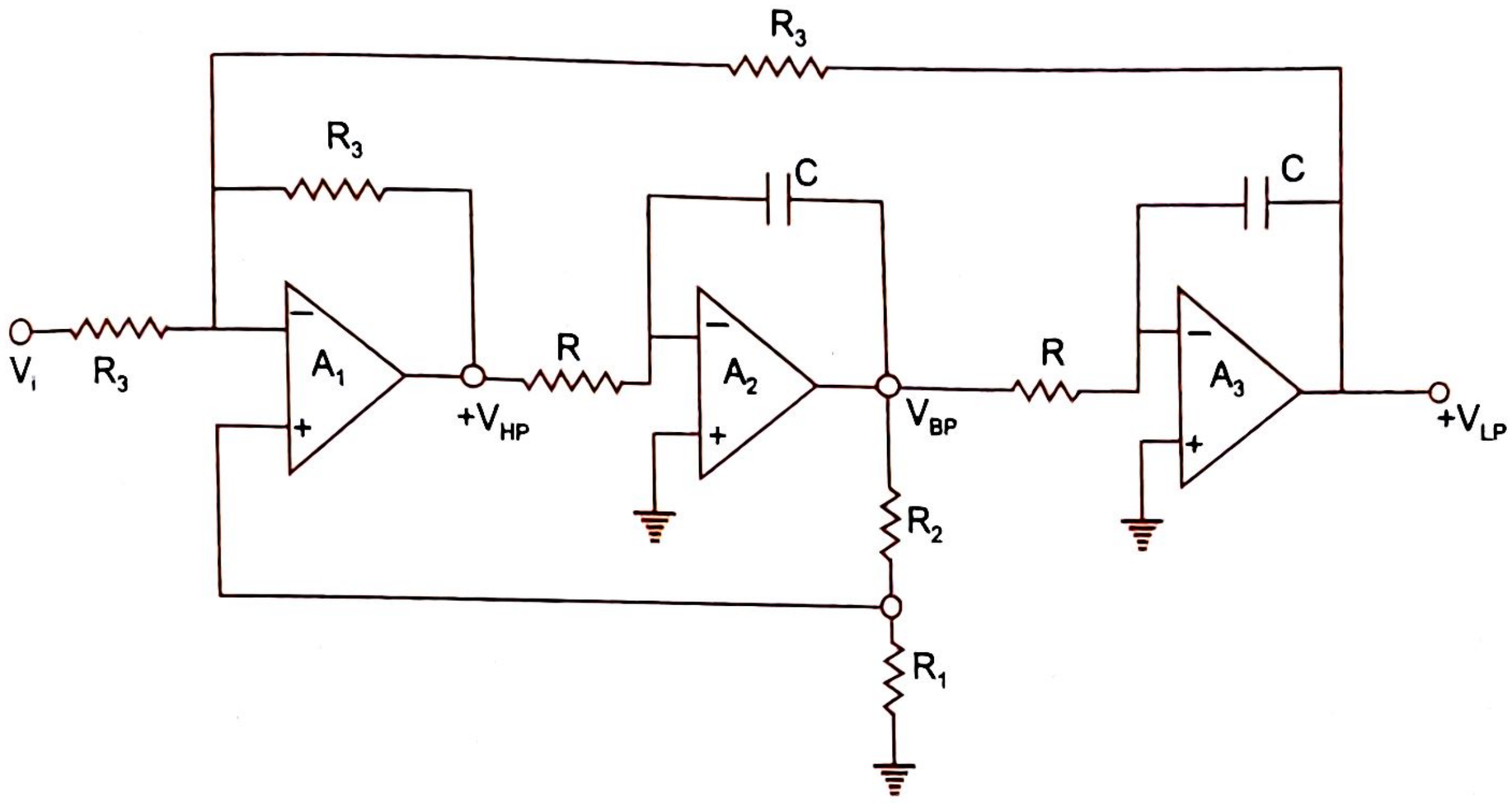


Fig. 7.21 (a) State variable filter

$$V_{BP} = -\frac{1}{RCs} V_{HP} \tag{7.94}$$

If $R = 1\ \text{M}\Omega$ and $C = 1\ \mu\text{F}$, so that $RC = 1$, we get,

$$V_{BP} = -\frac{1}{s} V_{HP} \tag{7.95}$$

Also for the inverting integrator A_3, we may write

$$V_{LP} = \frac{1}{s} V_{BP} = \frac{1}{s^2} V_{HP} \tag{7.96}$$

Op-amp A_1 is a three input summer. The output V_{HP} can be written using superposition theorem. That is,

$$V_{HP} = -\left(\frac{R_3}{R_3}\right) V_i - \left(\frac{R_3}{R_3}\right) V_{LP} + \left(1 + \frac{R_3}{R_3 \,||\, R_3}\right)\left(\frac{R_1}{R_1 + R_2}\right) V_{BP}$$

$$= -V_i - V_{LP} + 3\left(\frac{R_1}{R_1 + R_2}\right) V_{BP}$$

Put $$\alpha = 3\left(\frac{R_1}{R_1 + R_2}\right)$$

Then $$V_{HP} = -V_i - V_{LP} + \alpha\, V_{BP} \tag{7.97}$$

Eliminating V_{BP} and V_{LP} using Eqs. (7.95) and (7.96), we get

$$V_{HP} = -V_i - \frac{V_{HP}}{s^2} - \frac{\alpha}{s} V_{HP}$$

$$V_{HP}\left(1 + \frac{\alpha}{s} + \frac{1}{s^2}\right) = -V_i$$

So, the high pass transfer function H_{HP} is

$$H_{HP} = \frac{V_{HP}}{V_i} = \frac{-s^2}{s^2 + \alpha s + 1} \tag{7.98}$$

The damping factor α can be set by R_1 and R_2 for Bessel, Butterworth or Chebyshev response. Compare Eq. (7.98) to the standard high-pass transfer function of Eq. (7.36) as

$$\frac{A_o s^2}{s^2 + \alpha\omega_1 s + \omega_l^2} \tag{7.99}$$

So for the high-pass filter of the state variable filter,

$$A_o = -1 \text{ and } \omega_l = 1$$

The low-pass transfer function is obtained by eliminating V_{HP} and V_{BP} from Eq. (7.97) as

$$H_{LP} = \frac{V_{LP}}{V_i} = \frac{-1}{s^2 + \alpha s + 1} \tag{7.100}$$

As in High-pass filter, the low-pass filter has

$$A_o = -1, \ \omega_h = 1$$

and

$$\alpha = 3\left(\frac{R_1}{R_1 + R_2}\right)$$

Finally the band-pass impulse response is obtained from Eq. (7.97) by eliminating V_{HP} and V_{LP} as

$$H_{BP} = \frac{V_{BP}}{V_i} = \frac{s}{s^2 + \alpha s + 1} \tag{7.101}$$

The standard band-pass transfer function as given in Eq. (7.57) is

$$\frac{A_o \alpha \omega_o s}{s^2 + \alpha \omega_o s + \omega_o^2} \tag{7.102}$$

Comparing Eqs. (7.101) and (7.102), we get

$$A_o \alpha \omega_o = 1 \tag{7.103}$$

$$\omega_o = \frac{1}{RC} = 1, \ (RC \text{ has been assumed to be } 1) \tag{7.104}$$

therefore,

$$A_o = \frac{1}{\alpha} = \frac{R_1 + R_2}{3R_1} \tag{7.105}$$

From the analysis, we found that the band-pass response can be generated by integrating the high-pass response and that the low-pass is generated by integrating the band-pass.

The circuit of Fig. 7.21 (a) can be modified to that of Fig. 7.21 (b) where a fourth op-amp has been used to get a notch filter response. The op-amp A_4 provides the notch filter response by combining the low-pass and high-pass output. The notch filter output V_N is written as

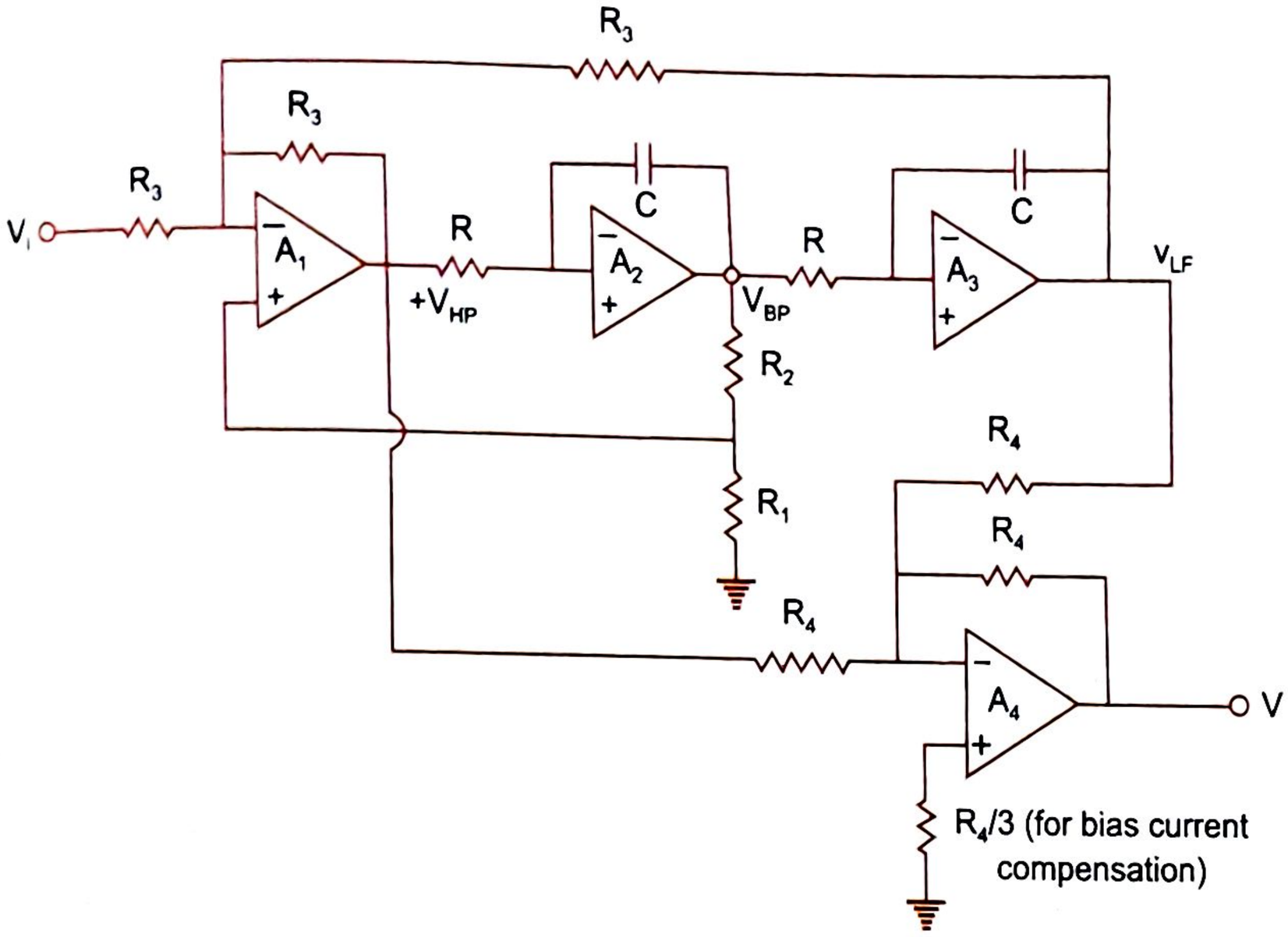


Fig. 7.21 (b) Four op-amp state variable filter with notch response

$$V_N = -\left(\frac{R_4}{R_4}\right)V_{HP} - \left(\frac{R_4}{R_4}\right)V_{LP} = -V_{HP} - V_{LP} \tag{7.106}$$

Putting the values of V_{HP} and V_{LP}, the transfer function of notch filter is obtained as

$$H_N = \frac{V_N}{V_i} = \frac{s^2+1}{s^2+\alpha s+1} \tag{7.107}$$

Thus it is possible to obtain LP, BP, HP and notch filter outputs from a state variable filter and therefore these are also known as universal filters. Quad op-amps such as LF347, TL074 and TLC274, FET input device are especially suited for these applications. With the advancement of IC technology, universal filters are available in single IC chip form. Datel's FLT-U2 and AF100 of National Semiconductor are the typical examples of IC universal filters.

State Variable Formulation

It may be noted that this filter is called state variable filter because the analog simulation can be made after the state variable formulation of the proper transfer function.

The band-pass filter transfer function of Eq. (7.57) can be rewritten for $A_0 = -1$, $\omega_0 = 1$, $\alpha = 1$ and assuming a dummy variable $X_1 = \mathcal{L}\, x_1(t)$, as

$$\frac{V_{BP}}{X_1}\cdot\frac{X_1}{V_i} = s\frac{1}{s^2+s+1} \tag{7.108}$$

Let

$$\frac{X_1}{V_i} = \frac{1}{s^2+s+1} \tag{7.109}$$

which can written in time domain as

$$\ddot{x}_1 + \dot{x}_1 + x_1 = v_i$$

Let $\dot{x}_1 = x_2$

then $\dot{x}_2 = -x_1 - x_2 + v_i$

These can be written in matrix form as

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -1 & -1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} v_i \tag{7.110}$$

and $$\frac{V_{BP}}{X_1} = s \tag{7.111}$$

leads to the output in time domain as $V_{BP} = \dot{x}_1 = x_2$

or, $$V_{BP} = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} \tag{7.112}$$

Similarly the high-pass transfer function H_{HP} of Eq. (7.98) with $\alpha = 1$ can be rewritten assuming another dummy variable $Y = \mathcal{L}y\,(t)$, as

$$H_{HP} = \frac{V_{HP}}{V_i} = -1 + \frac{s+1}{s^2+s+1} = -1 + \frac{Y}{V_i} \tag{7.113}$$

where $$\frac{Y}{V_i} = \frac{Y}{X_1} \cdot \frac{X_1}{V_i} = (s+1) \cdot \frac{1}{s^2+s+1} \tag{7.114}$$

Let $$\frac{X_1}{V_i} = \frac{1}{s^2+s+1} \tag{7.115}$$

It leads to

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -1 & -1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} v_i \tag{7.116}$$

and $$\frac{Y}{X_1} = (s+1) \tag{7.117}$$

leads to in time domain $y = \dot{x}_1 + x_1 = x_2 + x_1$

or, $$y = \begin{bmatrix} 1 & 1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} \tag{7.118}$$

Hence the output

$$V_{HP} = y - v_i = \begin{bmatrix} 1 & 1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} - (1)\, v_i \tag{7.119}$$

The simulation of Eqs. (7.116) and (7.119) is shown in Fig. 7.21 having V_{HP} as output. Similarly, the low-pass transfer function of Eq. (7.84) can be written in the same fashion as

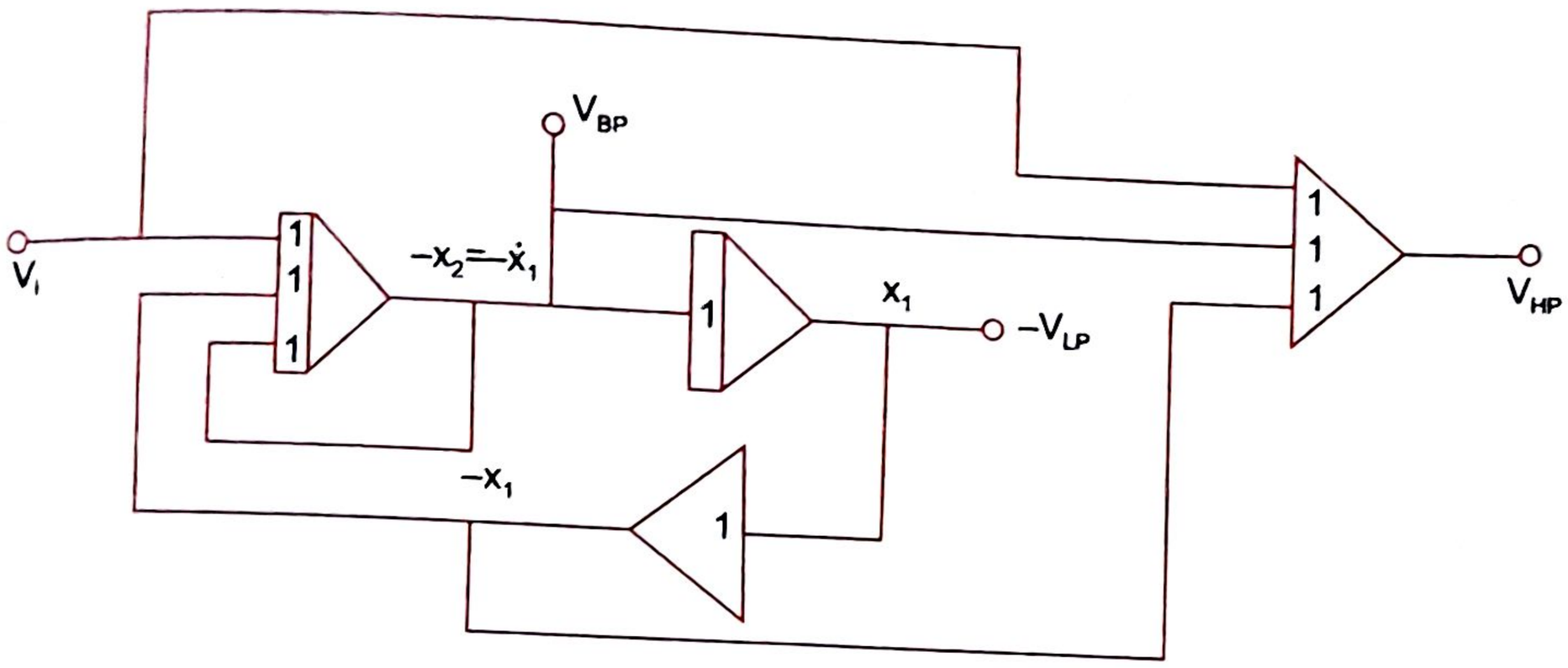


Fig. 7.22 Simulation of state variable filter

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -1 & -1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} v_i \tag{7.120}$$

and output

$$V_{LP} = \begin{bmatrix} -1 & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}$$

The simulation is as shown in Fig. 7.22.

9

555 TIMER

9.1 INTRODUCTION

The 555 timer is a highly stable device for generating accurate time delay or oscillation. Signetics Corporation first introduced this device as the SE555/NE555 and it is available in two package styles, 8-pin circular style, TO-99 can or 8-pin mini DIP or as 14-pin DIP. The 556 timer contains two 555 timers and is a 14-pin DIP. There is also available counter timer such as Exar's XR-2240 which contains a 555 timer plus a programmable binary counter in a single 16-pin package. A single 555 timer can provide time delay ranging from microseconds to hours whereas counter timer can have a maximum timing range of days.

The 555 timer can be used with supply voltage in the range of + 5V to + 18V and can drive load upto 200 mA. It is compatible with both TTL and CMOS logic circuits. Because of the wide range of supply voltage, the 555 timer is versatile and easy to use in various applications. Various applications include oscillator, pulse generator, ramp and square wave generator, mono-shot multivibrator, burglar alarm, traffic light control and voltage monitor etc.

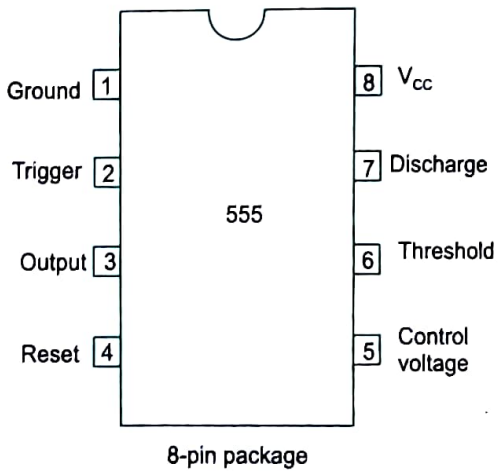


Fig. 9.1 Pin diagram

9.2 DESCRIPTION OF FUNCTIONAL DIAGRAM

Figure 9.1 gives the pin diagram and Fig. 9.2 gives the functional diagram for 555 IC timer. Referring to Fig. 9.2, three 5 kΩ internal resistors act as voltage divider, providing bias voltage of (2/3) V_{CC} to the upper comparator (UC) and (1/3) V_{CC} to the lower comparator (LC), where V_{CC} is the supply voltage. Since these two voltages fix the necessary comparator threshold voltage, they also aid in determining the timing interval. It is possible to vary time electronically too, by applying a modulation voltage to the control voltage input terminal (pin 5). In applications, where no such modulation is intended, it is recommended by manufacturers that a capacitor (0.01 μF) be connected between control voltage terminal (pin 5) and ground to by-pass noise or ripple from the supply.

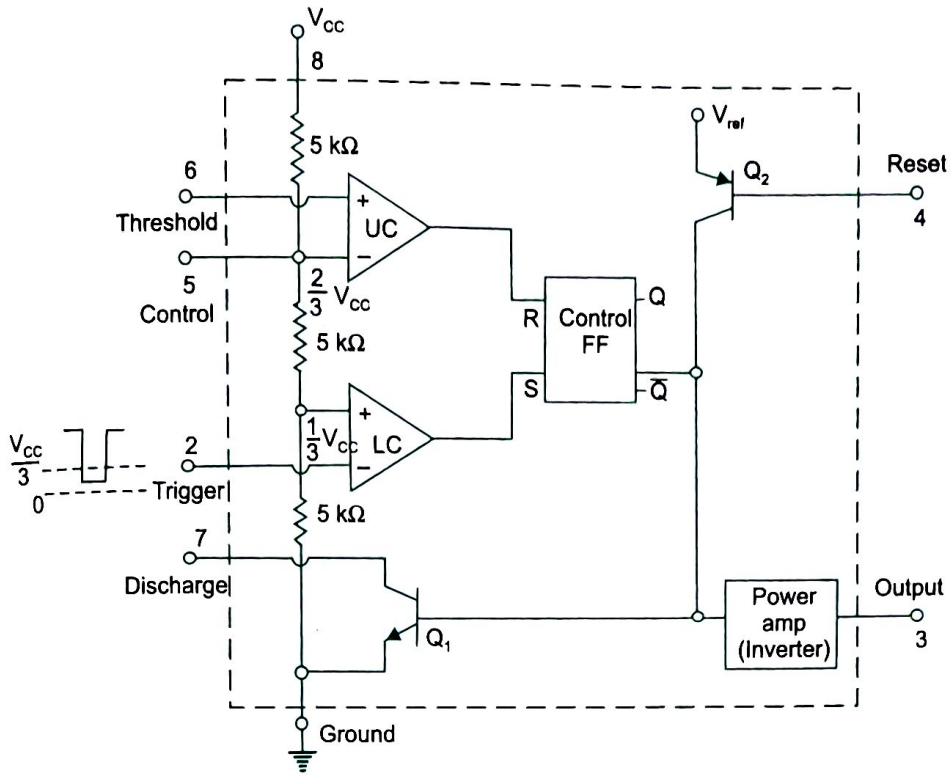


Fig. 9.2 Functional diagram of 555 timer

In the standby (stable) state, the output $\overline{Q}$ of the control flip-flop (FF) is HIGH. This makes the output LOW because of power amplifier which is basically an inverter. A negative going trigger pulse is applied to pin 2 and should have its dc level greater than the threshold level of the lower comparator (i.e. $V_{CC}/3$). At the negative going edge of the trigger, as the trigger passes through ($V_{CC}/3$), the output of the lower comparator goes HIGH and sets the FF ($Q = 1, \overline{Q} = 0$). During the positive excursion, when the threshold voltage at pin 6 passes through (2/3) V_{CC}, the output of the upper comparator goes HIGH and resets the FF ($Q = 0, \overline{Q} = 1$).

The reset input (pin 4) provides a mechanism to reset the FF in a manner which overrides the effect of any instruction coming to FF from lower comparator. This overriding reset is effective when the reset input is less than about 0.4 V. When this reset is not used, it is returned to V_{CC}. The transistor Q_2 serves as a buffer to isolate the reset input from the FF and transistor Q_1. The transistor Q_2 is driven by an internal reference voltage V_{ref} obtained from supply voltage V_{CC}.

9.3 MONOSTABLE OPERATION

Figure 9.3 shows a 555 timer connected for monostable operation and its functional diagram is shown in Fig. 9.4. In the standby state, FF holds transistor Q_1 ***on***, thus clamping the external timing capacitor C to ground. The output remains at ground potential, i.e. LOW. As the trigger passes through $V_{CC}/3$, the FF is set, i.e. $\overline{Q} = 0$. This makes the transistor Q_1 ***off*** and the short circuit across the timing capacitor C is released. As $\overline{Q}$ is LOW, output goes HIGH (= V_{CC}). The timing cycle now begins. Since C is unclamped, voltage across it rises exponentially through R towards V_{CC} with a time constant RC as in Fig. 9.5 (b). After

a time period T (calculated later), the capacitor voltage is just greater than (2/3) V_{CC} and the upper comparator resets the FF, that is, $R = 1$, $S = 0$ (assuming very small trigger pulse width). This makes $\bar{Q} = 1$, transistor Q_1 goes ***on*** (i.e. saturates), thereby discharging the capacitor C rapidly to ground potential. The output returns to the standby state or ground potential as shown in Fig. 9.5 (c).

The voltage across the capacitor as in Fig. 9.5 (b) is given by

$$v_c = V_{CC}\,(1 - e^{-t/RC}) \qquad (9.1)$$

At $t = T$, $\quad v_c = (2/3)\,V_{CC}$

Therefore, $\dfrac{2}{3}V_{CC} = V_{CC}\,(1 - e^{-T/RC})$

or, $\quad T = RC \ln (1/3)$

or, $\quad T = 1.1\,RC$ (seconds) $\qquad (9.2)$

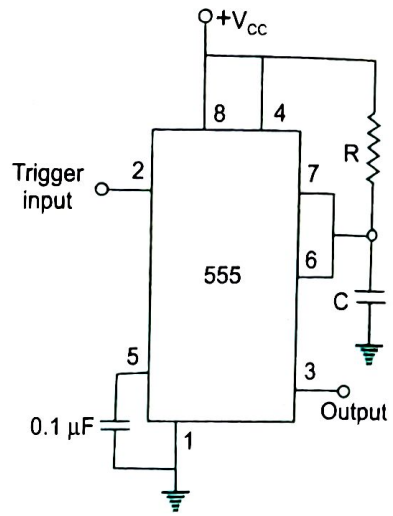


Fig. 9.3 Monostable multivibrator

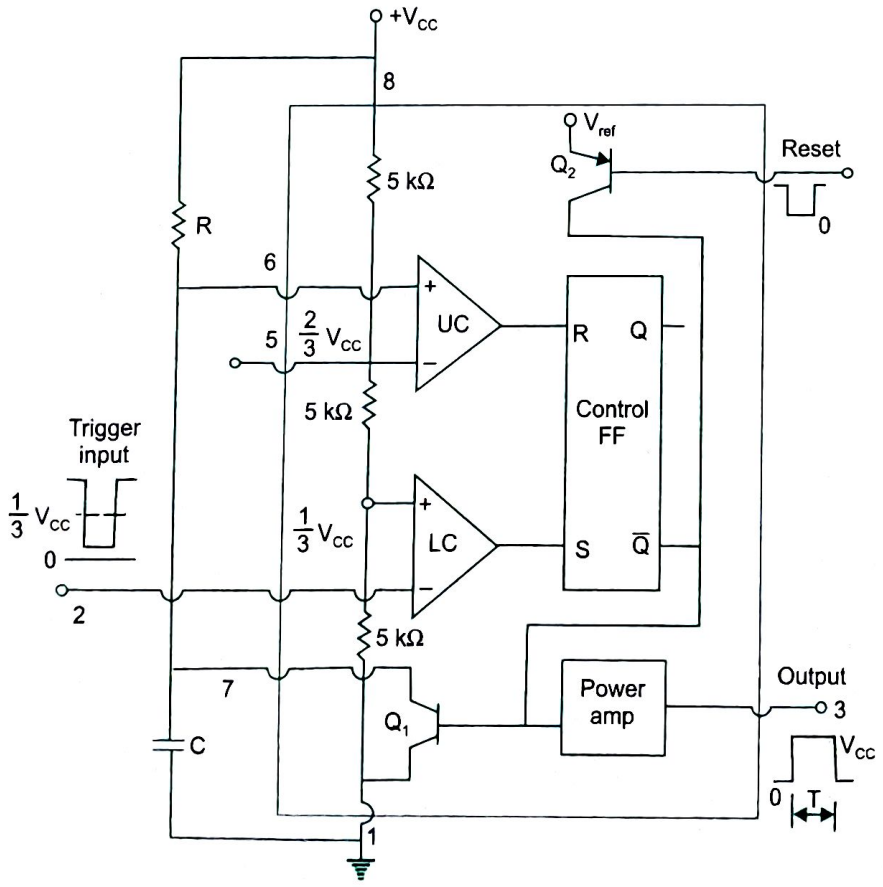


Fig. 9.4 Timer in monostable operation with functional diagram

It is evident from Eq. (9.2) that the timing interval is independent of the supply voltage. It may also be noted that once triggered, the output remains in the HIGH state until time T elapses, which depends only upon R and C. Any additional trigger pulse coming during this time will not change the output state. However, if a negative going reset pulse as in Fig. 9.5(d) is applied to the reset terminal (pin-4) during the timing cycle, transistor Q_2 goes ***off***, Q_1 becomes ***on*** and the external timing capacitor C is immediately discharged. The output now will be as in Fig. 9.5 (e). It may be seen that the output of Q_2 is connected directly to the input of Q_1 so as to turn ***on*** Q_1 immediately and thereby avoid the propagation delay through the FF. Now, even if the reset is released, the output will still remain LOW until

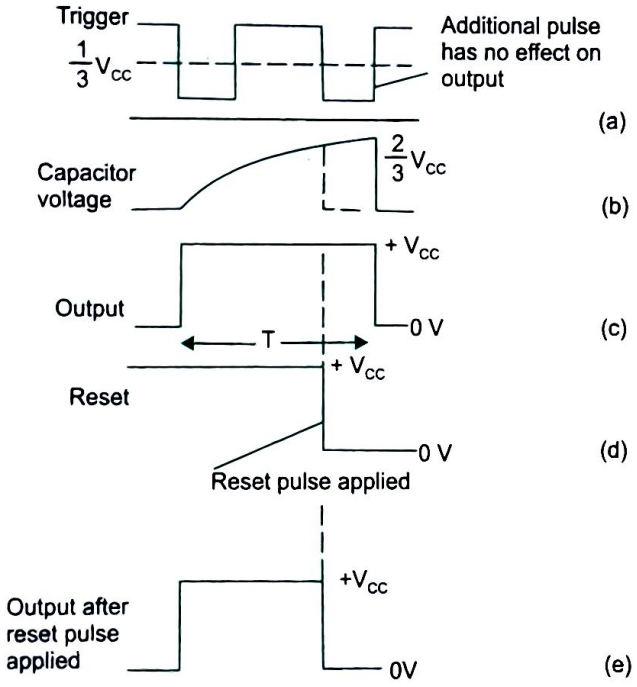


Fig. 9.5 Timing pulses

a negative going trigger pulse is again applied at pin 2. Figure 9.6 shows a graph of the various combinations of R and C necessary to produce a given time delay.

Sometimes the monostable circuit of Fig. 9.3 mistriggers on positive pulse edges, even with the control pin by pass capacitor. To prevent this, a modified circuit as shown in Fig. 9.7 is used. Here the resistor and capacitor combination of 10 kΩ and 0.001 μF at the input forms a differentiator. During the positive going edge of the trigger, diode D becomes forward biased, thereby limiting the amplitude of the positive spike to 0.7 V.

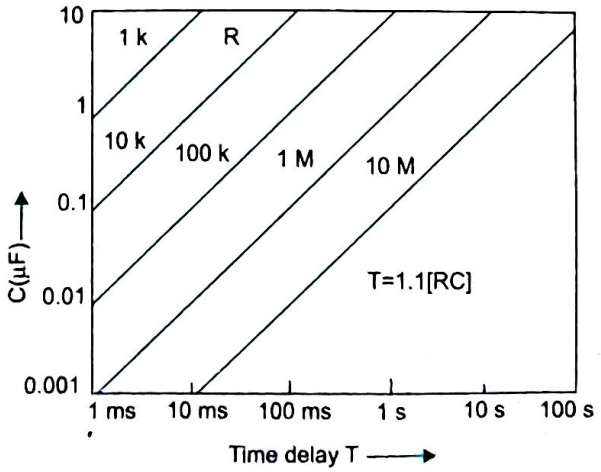


Fig. 9.6 Graph of *RC* combinations for different time delays

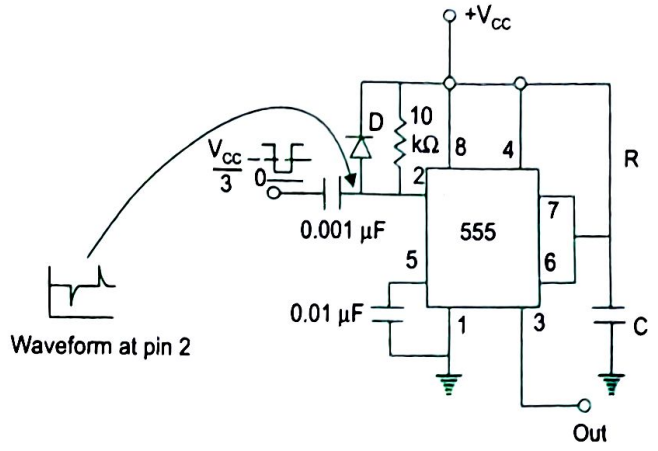


Fig. 9.7 Modified monostable circuit

Example 9.1

In the monostable multivibrator of Fig. 9.3, R = 100 kΩ and the time delay T = 100 mS. Calculate the value of C. Verify the value of C obtained from the graphs of Fig. 9.6.

Solution

From Eq. (9.2), we get

$$C = T/1.1\ R = 100 \times 10^{-3}/1.1 \times 100 \times 10^{3} = 0.9\ \mu F$$

From the graph of Fig. 9.6, the value of C is found to be 0.9 μF also.

9.3.1 Applications in Monostable Mode

Missing Pulse Detector

Missing pulse detector circuit using 555 timer is shown in Fig. 9.8. Whenever, input trigger is low, the emitter diode of the transistor Q is forward biased. The capacitor C gets clamped to few tenths of a volt (~ 0.7 V). The output of the timer goes HIGH. The circuit is designed so that the time period of the monostable circuit is slightly greater (1/3 longer) than that of the triggering pulses. So long the trigger pulse train keeps coming at pin 2, the output remains HIGH. However, if a pulse misses, the trigger input is high and transistor Q is cut

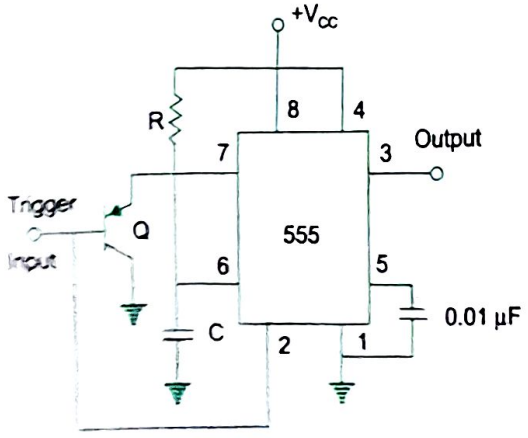


Fig. 9.8 A missing pulse detector monostable circuit

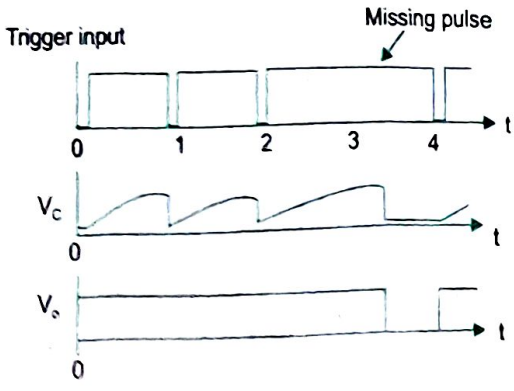


Fig. 9.9 Output of missing pulse detector

off. The 555 timer enters into normal state of monostable operation. The output goes LOW after time T of the mono-shot. Thus this type of circuit can be used to detect missing heartbeat. It can also be used for speed control and measurement. If input trigger pulses are generated from a rotating wheel, the circuit tells when the wheel speed drops below a predetermined value.

Linear Ramp Generator

Linear ramp can be generated by the circuit shown in Fig. 9.10. The resistor R of the monostable circuit is replaced by a constant current source. The capacitor is charged linearly by the constant current source formed by the transistor Q_3. The capacitor voltage v_c can be written as

$$v_c = \frac{1}{C}\int_0^t i\,dt \tag{9.3}$$

where i is the current supplied by the constant current source. Further, the KVL equation can be written as

$$\frac{R_1}{R_1 + R_2} V_{CC} - V_{BE} = (\beta + 1) I_B R_E \approx \beta I_B R_E = I_C R_E = i R_E \tag{9.4}$$

where I_B, I_C are the base current and collector current respectively, β is the current amplification factor in CE-mode and is very high. Therefore,

$$i = \frac{R_1 V_{CC} - V_{BE}(R_1 + R_2)}{R_E (R_1 + R_2)} \tag{9.5}$$

Now putting the value of the current i in Eq. 9.3, we get

$$v_c = \frac{R_1 V_{CC} - V_{BE}(R_1 + R_2)}{C R_E (R_1 + R_2)} \times t \tag{9.6}$$

At time $t = T$, the capacitor voltage v_c becomes (2/3) V_{CC}. Then we get

$$\frac{2}{3} V_{CC} = \frac{R_1 V_{CC} - V_{BE}(R_1 + R_2)}{R_E (R_1 + R_2) C} \times T \tag{9.7}$$

which gives the time period of the linear ramp generator as

$$T = \frac{(2/3) V_{CC} R_E (R_1 + R_2) C}{R_1 V_{CC} - V_{BE}(R_1 + R_2)} \tag{9.8}$$

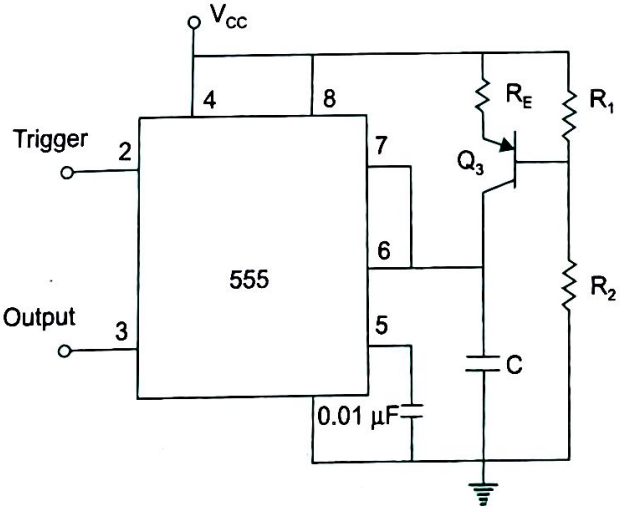


Fig. 9.10 Linear ramp generator

The capacitor discharges as soon as its voltage reaches (2/3) V_{CC} which is the threshold of the upper comparator in the monostable circuit functional diagram. The capacitor voltage remains zero till another trigger is applied. The various waveforms are shown in Fig. 9.11.

The practical values can be noted as

R_1 = 47 kΩ; R_2 = 100 kΩ; R_E = 2.7 kΩ; C = 0.1 μF.
V_{CC} = 5 V (any value between 5 to 18 V can be chosen)

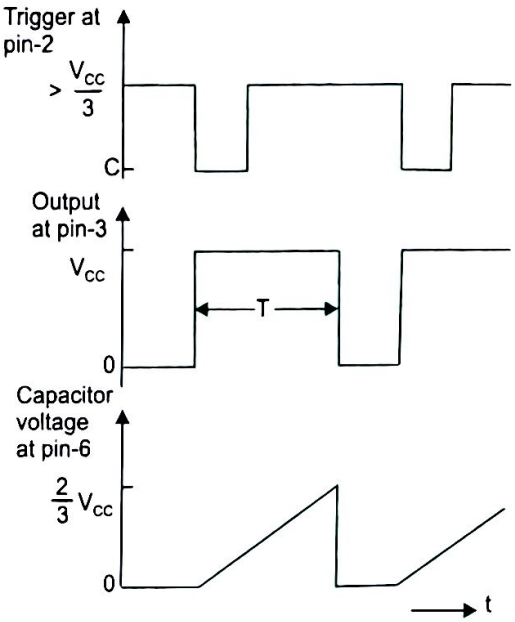


Fig. 9.11 Linear ramp generator output

Frequency Divider

A continuously triggered monostable circuit when triggered by a square wave generator can be used as a frequency divider, if the timing interval is adjusted to be longer than the period of the triggering square wave input signal. The monostable multivibrator will be triggered by the first negative going edge of the square wave input but the output will remain HIGH (because of greater timing interval) for next negative going edge of the input square wave as shown in Fig. 9.12. The mono-shot will however be triggered on the third negative going input, depending on the choice of the time delay. In this way, the output can be made integral fractions of the frequency of the input triggering square wave.

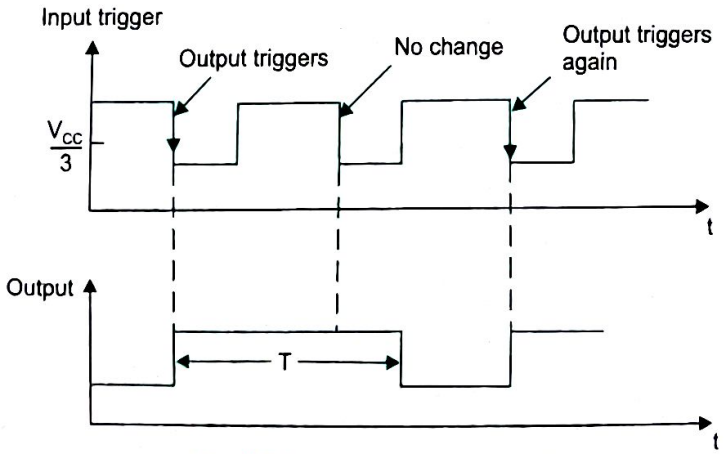


Fig. 9.12 Frequency divider circuit

Pulse Width Modulation

The circuit is shown in Fig. 9.13. This is basically a monostable multivibrator with a modulating input signal applied at pin-5. By the application of continuous trigger at pin-2, a series of output pulses are obtained, the duration of which depends on the modulating input at pin-5. The modulating signal applied at pin-5 gets superimposed upon the already existing voltage (2/3) V_{CC} at the inverting input terminal of UC. This in turn changes the threshold level of UC and the output pulse width modulation takes place. The modulating signal and the output waveform are shown in Fig. 9.14. It may be noted from the output waveform that the pulse duration, that is, the duty cycle only varies, keeping the frequency same as that of the continuous input pulse train trigger.

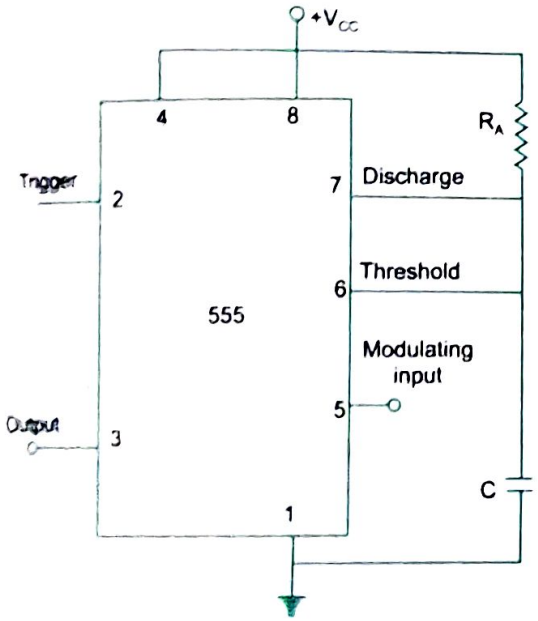


Fig. 9.13 Pulse width modulator

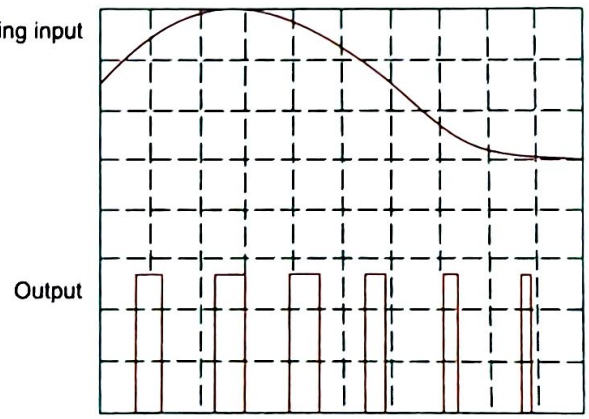


Fig. 9.14 Pulse width modulator waveforms

9.4 ASTABLE OPERATION

The device is connected for astable operation as shown in Fig. 9.15. For better understanding, the complete diagram of astable multivibrator with detailed internal diagram of 555 is shown in Fig. 9.16. Comparing with monostable operation, the timing resistor is now split into two sections R_A and R_B. Pin 7 of discharging transistor Q_1 is connected to the junction of R_A and R_B. When the power supply V_{CC} is connected, the external timing capacitor C charges towards V_{CC} with a time constant $(R_A + R_B)C$. During this time, output (pin 3) is high (equals V_{CC}) as Reset $R = 0$, Set $S = 1$ and this combination makes $\overline{Q} = 0$ which has unclamped the timing capacitor C.

When the capacitor voltage equals (to be precise is just greater than), (2/3) V_{CC} the upper comparator triggers the control flip-flop so that $\overline{Q} = 1$. This, in turn, makes transistor Q_1 *on* and capacitor C starts discharging towards ground through R_B and transistor Q_1 with a time constant R_BC (neglecting the forward resistance of Q_1). Current also flows into transistor Q_1 through R_A. Resistors R_A and R_B must be large enough to limit this current and prevent damage to the discharge transistor Q_1. The minimum value of R_A is approximately equal to $V_{CC}/0.2$ where 0.2 A is the maximum current through the *on* transistor Q_1.

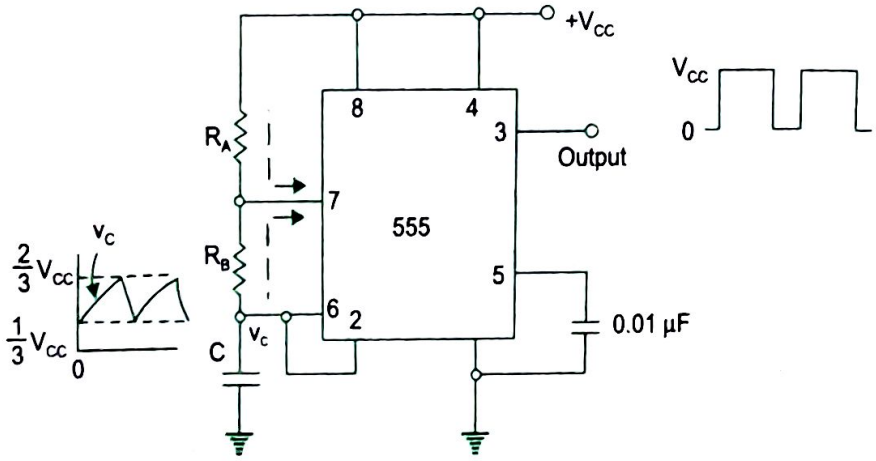


Fig. 9.15 Astable multivibrator using 555 timer

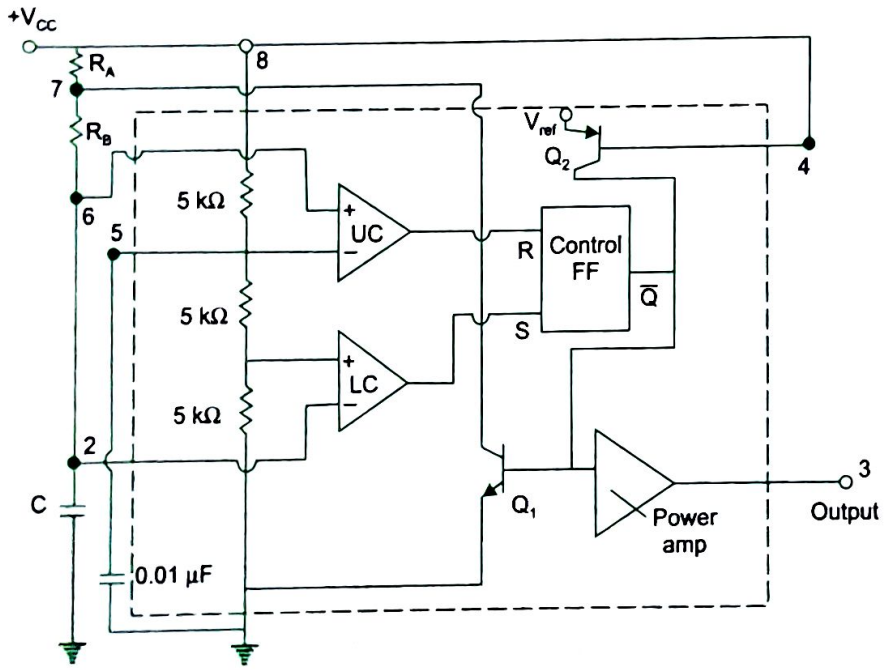


Fig. 9.16 Functional diagram of astable multivibrator using 555 timer

During the discharge of the timing capacitor C, as it reaches (to be precise, is just less than) $V_{CC}/3$, the lower comparator is triggered and at this stage $S = 1$, $R = 0$, which turns $\overline{Q} = 0$. Now $\overline{Q} = 0$ unclamps the external timing capacitor C. The capacitor C is thus periodically charged and discharged between (2/3) V_{CC} and (1/3) V_{CC} respectively. Figure 9.17 shows the timing sequence and capacitor voltage wave form. The length of time that the output remains HIGH is the time for the capacitor to charge from (1/3) V_{CC} to (2/3) V_{CC}. It may be calculated as follows:

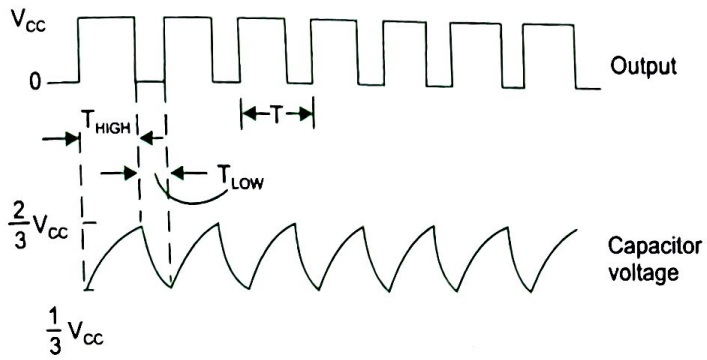


Fig. 9.17 Timing sequence of astable multivibrator

The capacitor voltage for a low pass RC circuit subjected to a step input of V_{CC} volts is given by

$$v_c = V_{CC}(1 - e^{-t/RC})$$

The time t_1 taken by the circuit to charge from 0 to (2/3) V_{CC} is,

$$(2/3)\, V_{CC} = V_{CC}(1 - e^{-t_1/RC}) \tag{9.9}$$

or, $$t_1 = 1.09\, RC$$

and the time t_2 to charge from 0 to (1/3) V_{CC} is,

$$(1/3)\, V_{CC} = V_{CC}(1 - e^{-t_2/RC}) \tag{9.10}$$

or, $$t_2 = 0.405\, RC$$

So the time to charge from (1/3) V_{CC} to (2/3) V_{CC} is

$$t_{HIGH} = t_1 - t_2$$

$$t_{HIGH} = 1.09\, RC - 0.405\, RC = 0.69\, RC$$

So, for the given circuit,

$$t_{HIGH} = 0.69\,(R_A + R_B)C \tag{9.11}$$

The output is low while the capacitor discharges from (2/3) V_{CC} to (1/3) V_{CC} and the voltage across the capacitor is given by

$$(1/3)\, V_{CC} = (2/3) V_{CC}\, e^{-t/RC}$$

Solving, we get $t = 0.69\, RC$

So, for the given circuit, $t_{LOW} = 0.69\, R_B C$ (9.12)

Notice that both R_A and R_B are in the charge path, but only R_B is in the discharge path. Therefore, total time,

$$T = t_{HIGH} + t_{LOW}$$

or, $$T = 0.69\,(R_A + 2R_B)\, C$$

So, $$f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C} \tag{9.13}$$

Chapter 9

Figure 9.18 shows a graph of the various combinations of $(R_A + 2R_B)$ and C necessary to produce a given stable output frequency. The duty cycle D of a circuit is defined as the ratio of ON time to the total time period $T = (t_{ON} + t_{OFF})$. In this circuit, when the transistor Q_1 is ***on***, the output goes low. Hence,

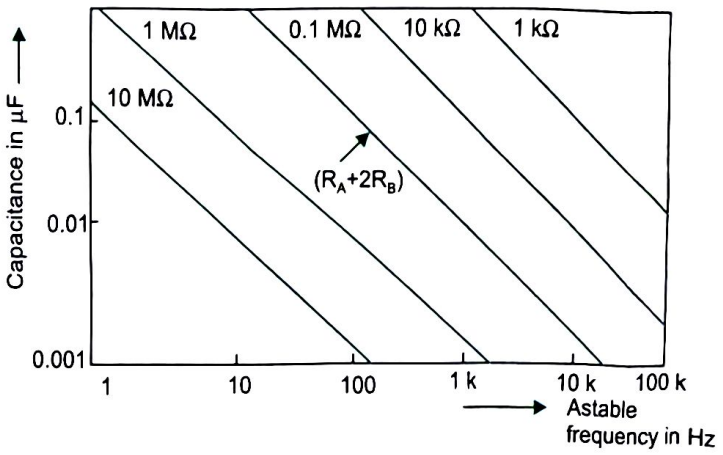


Fig. 9.18 Frequency dependence of R_A, R_B and C

$$D\% = \frac{t_{LOW}}{T} \times 100$$

$$= \frac{R_B}{R_A + 2R_B} \times 100 \qquad (9.14)$$

With the circuit configuration of Fig. 9.15 it is not possible to have a duty cycle more than 50% since $t_{HIGH} = 0.69\ (R_A + R_B)\ C$ will always be greater than $t_{LOW} = 0.69\ R_B\ C$. In order to obtain a symmetrical square wave i.e. $D = 50\%$, the resistance R_A must be reduced to zero. However, now pin 7 is connected directly to V_{CC} and extra current will flow through Q_1 when it is ***on***. This may damage Q_1 and hence the timer.

An alternative circuit which will allow duty cycle to be set at practically any level is shown in Fig. 9.19. During the charging portion of the cycle, diode D_1 is forward biased effectively short circuiting R_B so that

$$t_{HIGH} = 0.69\ R_A C$$

However, during the discharging portion of the cycle, transistor Q_1 becomes ON, thereby grounding pin 7 and hence the diode D_1 is reverse biased.

So $t_{LOW} = 0.69\ R_B\ C$ (9.15)

$$T = t_{HIGH} + t_{LOW} = 0.69\ (R_A + R_B)\ C \qquad (9.16)$$

or, $$f = \frac{1.45}{(R_A + R_B)C} \qquad (9.17)$$

and duty cycle $D = \dfrac{R_B}{R_A + R_B}$

Resistors R_A and R_B could be made variable to allow adjustment of frequency and pulse width. However, a series resistor of atleast 100 Ω (fixed) should be added to each R_A and R_B. This will limit peak current to the discharge transistor Q_1 when the variable resistors are at minimum value. And, if R_A is made equal to R_B, then 50% duty cycle is achieved.

Symmetrical square wave generator by adding a clocked JK flip-flop to the output of the nonsymmetrical square wave generator is

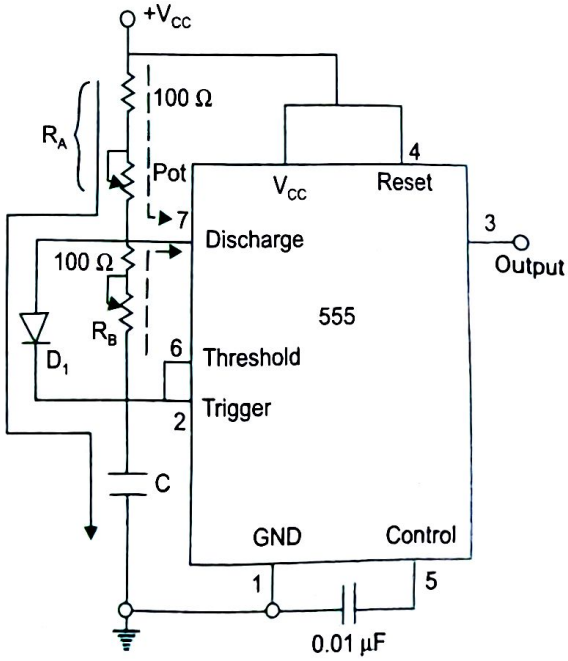


Fig. 9.19 Adjustable duty cycle rectangular wave generator

shown in Fig. 9.20. The clocked flip-flop acts as binary divider to the timer output. The output frequency in this case will be one half that of the timer. The advantage of this circuit is of having output of 50% duty cycle without any restriction on the choice of R_A and R_B.

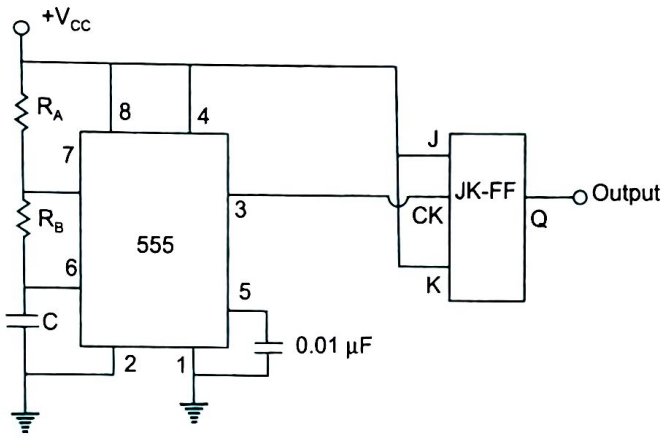


Fig. 9.20 Symmetrical waveform generator

Example 9.2

Refer Fig. 9.15. For $R_A = 6.8\ k\Omega$, $R_B = 3.3\ k\Omega$ and $C = 0.1\ \mu F$, calculate (a) t_{HIGH} (b) t_{LOW} (c) free running frequency (d) duty cycle, D.

Solution

(a) By Eq. (9.11)

$$t_{HIGH} = 0.69\,(6.8\ k\Omega + 3.3\ k\Omega)\,(0.1\ \mu F) = 0.7\ ms$$

(b) By Eq. (9.12)

$$t_{LOW} = 0.69\,(3.3\ k\Omega)\,(0.1\ \mu F) = 0.23\ ms$$

(c) $$f = \frac{1.45}{[(6.8\ k\Omega) + (2)(3.3\ k\Omega)](0.1\ \mu F)} = 1.07\ kHz$$

(d) $$D = \frac{t_{LOW}}{T} = \frac{R_B}{R_A + 2R_B}$$

$$= \frac{3.3\ k\Omega}{6.8\ k\Omega + 2(3.3\ k\Omega)} = 0.25\ or, 25\%$$

9.4.1 Applications in Astable Mode

FSK Generator

In digital data communication, binary code is transmitted by shifting a carrier frequency between two preset frequencies. This type of transmission is called frequency shift keying (FSK) technique. A 555 timer in astable mode can be used to generate FSK signal. The circuit is as shown in Fig. 9.21. The standard digital data input frequency is 150 Hz. When input is HIGH, transistor Q is ***off*** and 555 timer works in the normal astable mode of operation. The frequency of the output waveform given by Eq. (9.1) can be rewritten as

$$f_o = \frac{1.45}{(R_A + 2R_B)C} \tag{9.18}$$

In a tele-typewriter using a modulator-demodulator (MODEM), a frequency between 1070 Hz to 1270 Hz is used as one of the standard FSK signals. The components R_A and R_B and the capacitor C can be selected so that f_o is 1070 Hz.

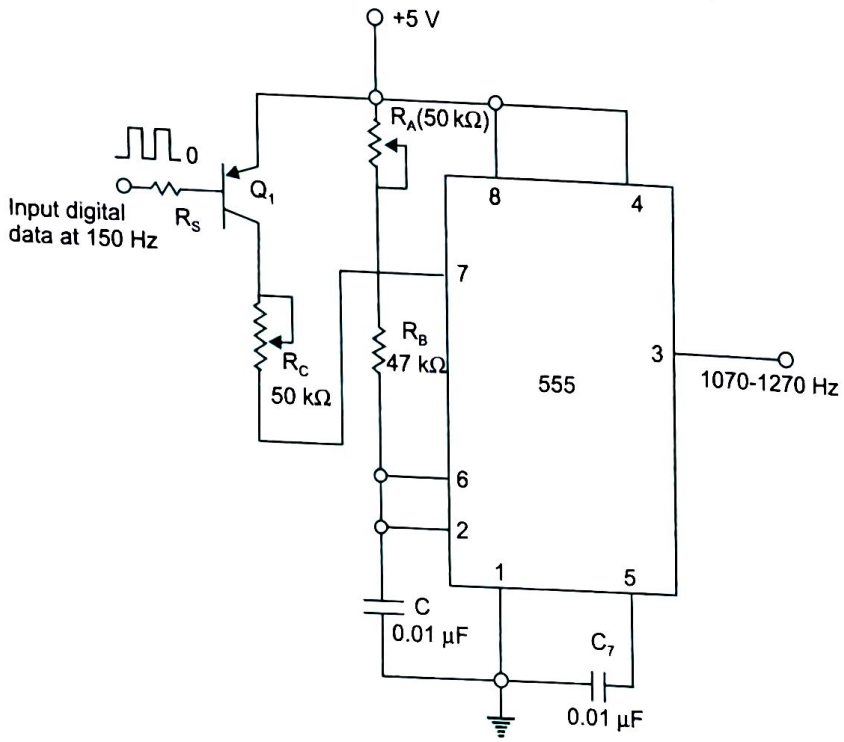


Fig. 9.21 FSK generator

When the input is LOW, Q goes ***on*** and connects the resistance R_C across R_A. The output frequency is now given by

$$\frac{1.45}{(R_A \| R_C) + 2R_B} \tag{9.19}$$

The resistance R_C can be adjusted to get an output frequency 1270 Hz.

Pulse-Position Modulator

The pulse-position modulator can be constructed by applying a modulating signal to pin 5 of a 555 timer connected for astable operation as shown in Fig. 9.22. The output pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied.

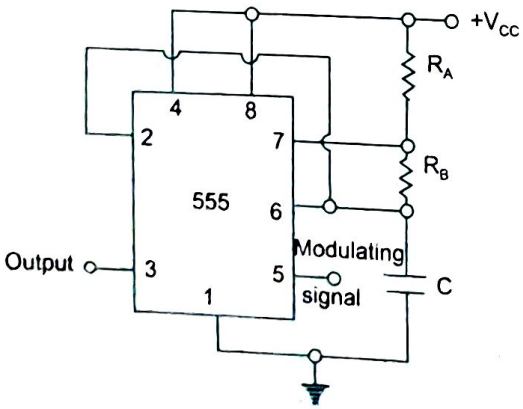


Fig. 9.22 Pulse position modulator

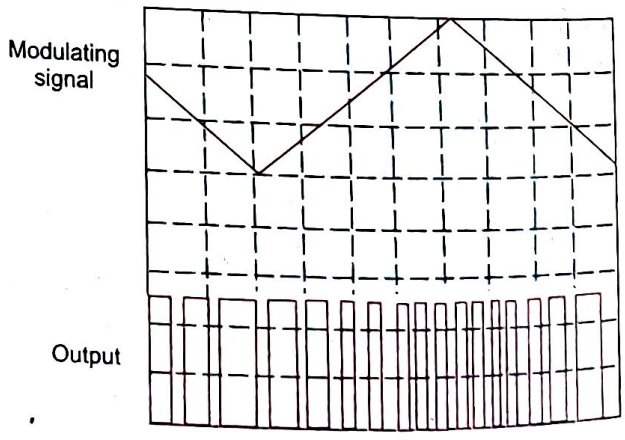


Fig. 9.23 Pulse position modulator output

Figure 9.23 shows the output waveform generated for a triangle wave modulation signal. It may be noted from the output waveform that the frequency is varying leading to pulse position modulation. The typical practical component values may be noted as

R_A = 3.9 kΩ, R_B = 3 kΩ, C = 0.01 μF

V_{CC} = 5 V (any value between 5 V to 18 V may be chosen)

9.5 SCHMITT TRIGGER

The use of 555 timer as a Schmitt Trigger is shown in Fig. 9.24. Here the two internal comparators are tied together and externally biased at $V_{CC}/2$ through R_1 and R_2. Since the upper comparator will trip at (2/3) V_{CC} and lower comparator at (1/3) V_{CC}, the bias provided by R_1 and R_2 is centered within these two thresholds.

Thus, a sine wave of sufficient amplitude (> $V_{CC}/6 = 2/3\ V_{CC} - V_{CC}/2$) to exceed the reference levels causes the internal flip-flop to alternately set and reset, providing a square wave output as shown in Fig. 9.25.

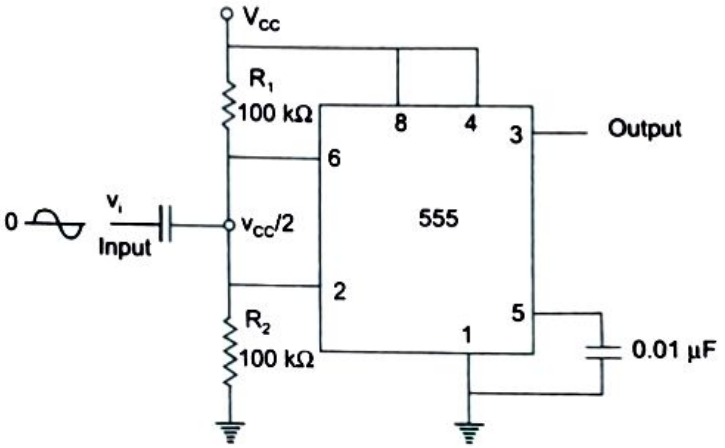


Fig. 9.24 Timer in Schmitt Trigger Operation

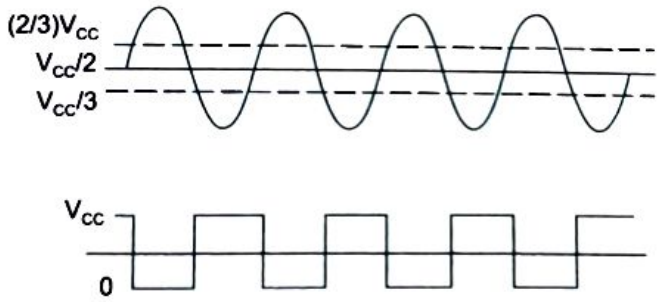


Fig. 9.25 Input output waveforms of Schmitt Trigger

It may be noted that unlike conventional multivibrator, no frequency division is taking place and frequency of square wave remains the same as that of input signal.

SUMMARY

1. 555 IC Timer can produce very accurate and stable time delays, from microseconds to hours.
2. Timer is available in two packages, circular can and DIP.
3. It can be used with supply voltage varying from 5 to 18 V and thus is compatible with TTL and CMOS circuits.
4. Timer can be used in monostable or astable mode of operation. Its various applications include waveform generator, missing pulse detector, frequency divider, pulse width modulator, burglar alarm, FSK generator, ramp generator, pulse position modulator etc.

REVIEW QUESTIONS

9.1. Draw and explain the functional diagram of a 555 Timer.
9.2. Explain the function of reset.
9.3. What are the modes of operation of a timer?
9.4. Derive the expression of time delay of a monostable multivibrator.
9.5. Discuss some applications of timer in monostable mode.
9.6. Define duty cycle D.
9.7. Give methods for obtaining symmetrical square wave.
9.8. Discuss the operation of a FSK generator using 555 timer.
9.9. How is an astable multivibrator connected into a pulse position modulator?
9.10. Draw the circuit of a Schmitt trigger using 555 timer and explain its operation.

PROBLEMS

9.1. Design a monostable multivibrator using 555 timer to produce a pulse width of 100 ms. Verify the values of R and C obtained from the graph of Fig. 9.6.
9.2. The monostable multivibrator of Fig. 9.3 is used as a divide-by-3 network. The frequency of the input trigger is 15 kHz. If the value of C = 0.01 μF, calculate, the value of resistance R.
9.3. In the astable multivibrator of Fig. 9.15, R_A = 2.2 kΩ, R_B = 6.8 kΩ and C = .01 μF. Calculate (i) t_{HIGH} (ii) t_{LOW}, (iii) free running frequency, and (iv) duty cycle D.
9.4. Design a square waveform generator of frequency 100 Hz and duty cycle of 75%.
9.5. Design a symmetrical square waveform generator of 10 kHz.

EXPERIMENT

To construct and observe the waveforms of a 1 kHz square waveform generator using 555 timer for duty cycle, (a) D = 0.25; (b) D = 0.50.

Design Aspects:

(a) Unsymmetrical square waveform generator

$$f = 1 \text{ kHz and } D = 0.25$$

In Fig. 9.15, $$f = \frac{1.45}{(R_A + 2R_B)C}$$

and $$D = \frac{R_B}{R_A + 2R_B}$$

Select $C = 0.1$ μF

Solving for R_A and R_B, we get

$$R_A = 3.6 \text{ kΩ}; \; R_B = 5.5 \text{ kΩ}$$

(b) Symmetrical square waveform generator

$$f = 1 \text{ kHz and } D = 0.50$$

In the circuit of Fig. 9.19

$$f = \frac{1.45}{(R_A + R_B)C}$$

and $$D = \frac{R_B}{R_A + R_B}$$

Select $C = 0.1\ \mu F$

Use a diode 0A79

Solve for R_A and R_B. We get.

$$R_A = R_B = 7.25\ k\Omega$$

PROCEDURE

1. Connect the circuit of Fig. 9.15 using component values as obtained in design part (a).
2. Observe and sketch the capacitor voltage waveform (pin-6) and output waveform (pin-3). Measure the frequency and duty cycle of the output waveform.
3. Next make the circuit of Fig. 9.19 using component values as obtained from design part (b).
4. Repeat step 2.

10

PHASE-LOCKED LOOPS

10.1 INTRODUCTION

The phase-locked loop (PLL) is an important building block of linear systems. Electronic phase-locked loop (PLL) came into vogue in the 1930s when it was used for radar synchronisation and communication applications. The high cost of realizing PLL in discrete form limited its use earlier. Now with the advanced IC technology, PLLs are available as inexpensive monolithic ICs. This technique for electronic frequency control is used today in satellite communication systems, air borne navigational systems, FM communication systems, computers etc. The basic principle of PLL, different ICs and important applications are discussed.

10.2 BASIC PRINCIPLES

The basic block schematic of the PLL is shown in Fig. 10.1. This feedback system consists of:

1. Phase detector/comparator
2. A low pass filter
3. An error amplifier
4. A Voltage Controlled Oscillator (VCO).

The VCO is a free running multivibrator and operates at a set frequency f_o called free running frequency. This frequency is determined by an external timing capacitor and an external resistor. It can also be shifted to either side by applying a dc control voltage v_c to an appropriate terminal of the IC. The frequency deviation is directly proportional to the dc control voltage and hence it is called a "Voltage Controlled Oscillator" or, in short, VCO.

If an input signal v_s of frequency f_s is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output v_o of the VCO. If the two signals differ in frequency and/or phase, an error voltage v_e is generated. The phase detector is basically a multiplier and produces the sum $(f_s + f_o)$ and difference $(f_s - f_o)$ components at its output. The high frequency component $(f_s + f_o)$ is removed by the low pass filter and the difference frequency component is amplified and then applied as control voltage v_c to VCO. The signal v_c shifts the VCO frequency in a direction to reduce the frequency difference between f_s and f_o. Once this action starts, we say that the signal is in the capture range. The VCO continues to change frequency till its output frequency is exactly the same as the input signal

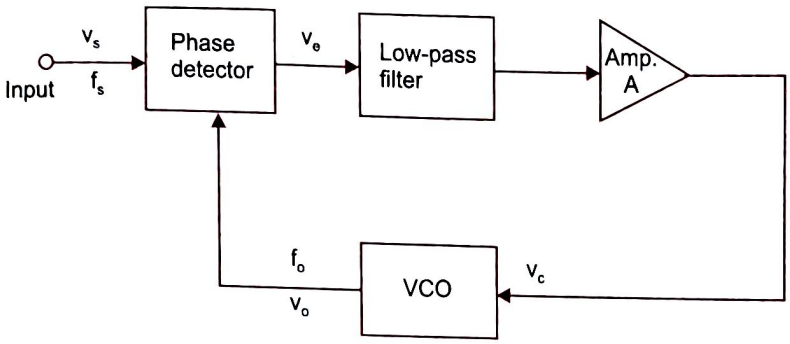


Fig. 10.1 Block schematic of the PLL

frequency. The circuit is then said to be locked. Once locked, the output frequency f_o of VCO is identical to f_s except for a finite phase difference ϕ. This phase difference ϕ generates a corrective control voltage v_c to shift the VCO frequency from f_o to f_s and thereby maintain the lock. Once locked, PLL tracks the frequency changes of the input signal. Thus, a PLL goes through three stages (i) free running, (ii) capture and (iii) locked or tracking.

Figure 10.2 shows the capture transient. As capture starts, a small sine wave appears. This is due to the difference frequency between the VCO and the input signal. The dc component of the beat drives the VCO towards the lock. Each successive cycle causes the VCO frequency to move closer to the input signal frequency. The difference in frequency becomes smaller and a large dc component is passed by the filter, shifting the VCO frequency further. The process continues until the VCO locks on to the signal and the difference frequency is dc.

The low pass filter controls the capture range. If VCO frequency is far away, the beat frequency will be too high to pass through the filter and the PLL will not respond. We say that the signal is out of the capture band. However, once locked, the filter no longer restricts the PLL. The VCO can track the signal well beyond the capture band. Thus tracking range is always larger than the capture range.

Some of the important definitions in relation to PLL are:

Lock-in Range: Once the PLL is locked, it can track frequency changes in the incoming signals. The range of frequencies over which the PLL can maintain lock with the incoming signal is called the lock-in range or tracking range. The lock range is usually expressed as a percentage of f_o, the VCO frequency.

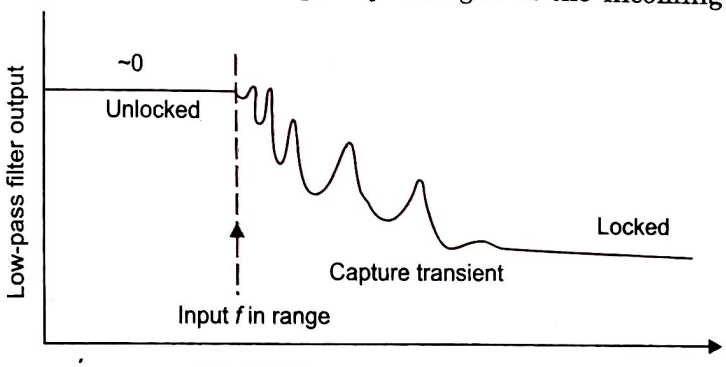


Fig. 10.2 The capture transient

Capture Range: The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. This parameter is also expressed as percentage of f_o.

Pull-in time: The total time taken by the PLL to establish lock is called pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

10.3 PHASE DETECTOR/COMPARATOR

The phase detection is the most important part of the PLL system. There are two types of phase detectors used, analog and digital.

10.3.1 Analog Phase Detector

The principle of analog phase detection using switch type phase detector is shown in Fig. 10.3(a). An electronic switch S is opened and closed by signal coming from VCO (normally a square wave) as shown in Fig. 10.3 (b). The input signal is, therefore, chopped at a repetition rate determined by VCO frequency. Figure 10.3 (c) shows the input signal v_s assumed to be in phase ($\phi = 0°$) with

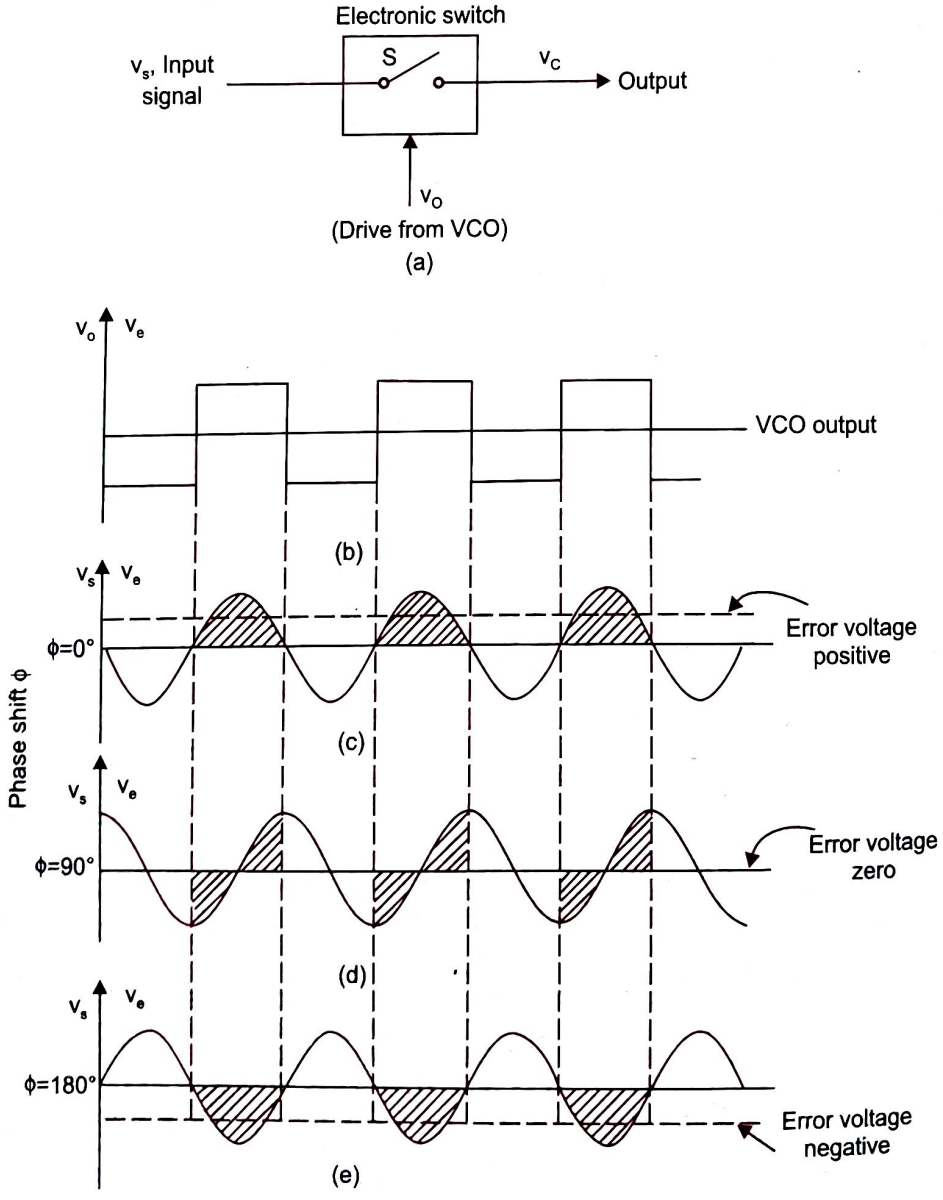


Fig. 10.3 Phase detector for PLL (a) Basic scheme (b) VCO output waveform. Input and output waveform (hatched) of phase detector for (c) $\phi = 0$ (d) $\phi = 90°$ (e) $\phi = 180°$

VCO output v_o. Since the switch S is closed only when VCO output is positive, the output waveform v_e will be half sinusoids (shown hatched). Similarly, the output waveform for $\phi = 90°$ and $\phi = 180°$ is shown in Fig. 10.3 (d, e). This type of phase detector is called a half wave detector, since the phase information for only one-half of the input waveform is detected and averaged. The output of the phase comparator when filtered through a low pass filter gives an error signal which is the average value of the output waveform shown by dotted line in Fig. 10.3 (c, d, e).

It may be seen that the error voltage is zero when the phase shift between the two inputs is 90°. So, for perfect lock, the VCO output should be 90° out of phase with respect to the input signal.

Analysis

A phase comparator is basically a multiplier which multiplies the input signal ($v_s = V_s \sin 2\pi f_s t$) by the VCO signal ($v_o = V_o \sin (2\pi f_o t + \phi)$). Thus the phase comparator output is,

$$v_e = KV_sV_o \sin (2\pi f_s t) \sin (2\pi f_o t + \phi) \tag{10.1}$$

where K is the phase comparator gain (or attenuation constant) and ϕ is the phase shift between the input signal and the VCO output. Equation 10.1 can be simplified as,

$$v_e = \frac{KV_sV_o}{2}\left[\cos(2\pi f_s t - 2\pi f_o t - \phi) - \cos(2\pi f_s t + 2\pi f_o t + \phi)\right] \tag{10.2}$$

when at lock, that is, $f_s = f_o$,

$$\text{Then } v_e = \frac{KV_sV_o}{2}\left[\cos(-\phi) - \cos(2\pi \times 2f_o t + \phi)\right] \tag{10.3}$$

This shows that the phase comparator output contains a double frequency term and a dc term $(KV_sV_o/2) \cos \phi$ which varies as a function of phase ϕ, that is, $\cos \phi$ between the two signals. The double frequency term is eliminated by the low pass filter and the dc signal is applied to the modulating input terminal of a VCO. It can be seen that in the perfect locked state ($f_s = f_o$), the phase shift should be 90° ($\cos 90° = 0$), in order to get zero error signal, that is, $v_e = 0$.

There are two problems associated with the switch type phase detector:

1. The output voltage v_e is proportional to the input signal amplitude V_s. This is undesirable since it makes phase detector gain and the loop gain dependent on the input signal amplitude.
2. The output is proportional to $\cos \phi$ and not proportional to ϕ making it non-linear.

Both these problems can be eliminated by limiting the amplitude of the input signal, that is, converting the input to a constant amplitude square wave. A circuit which performs phase comparison with square wave input is shown in Fig. 10.4 (a). This is a balanced modulator used as full-wave switching phase detector. Here the input signal is applied to the differential pair Q_1Q_2. Transistors Q_3–Q_4 and Q_5–Q_6 are two sets of SPDT switches activated by the VCO output. The input signal v_s and the VCO output v_o are assumed to be high enough to switch the transistors in Fig. 10.4 (a) fully ***on*** or ***off***. In Fig. 10.4 (b) when v_s and v_o both are high during the time 0 to $(\pi-\phi)$, transistors Q_1 and Q_3 are driven ***on*** and current I_E flows through Q_1 and Q_3. This gives an output voltage

$$v_e = -I_E R_L \tag{10.4}$$

Next for the period $(\pi - \theta)$ for π, when v_s is high and v_o is low, transistors Q_1 and Q_4 are driven ***on*** resulting in an output voltage

$$v_e = I_E R_L \tag{10.5}$$

In this way, the output voltage waveform v_e in Fig. 10.4 (b) is obtained.

The average value of the phase detector output v_e can be calculated as,

$$(v_e)_{av} = \frac{1}{\pi}[(\text{area } A_1) + (\text{area } A_2)]$$

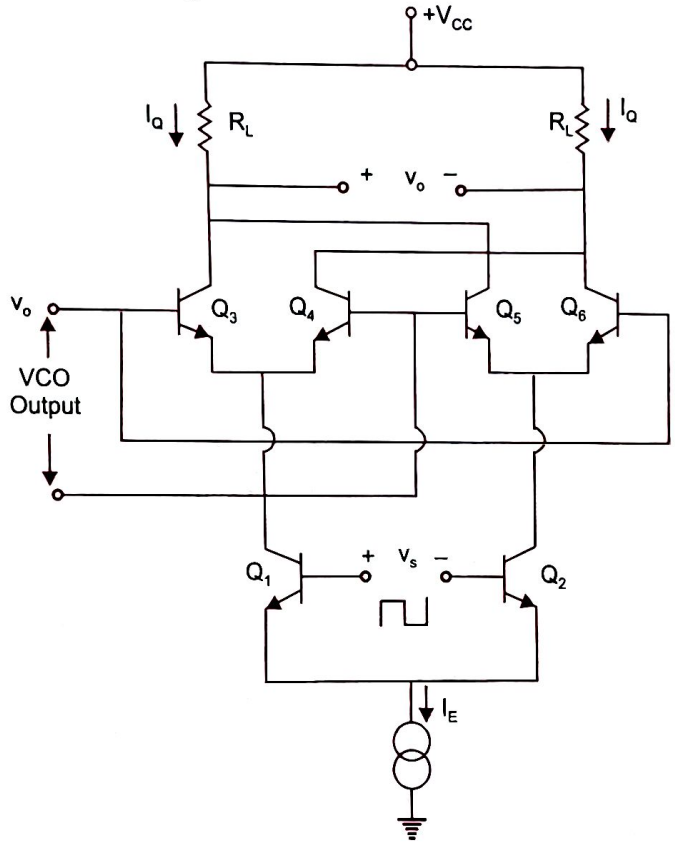


Fig. 10.4 (a) Phase detector for IC PLL

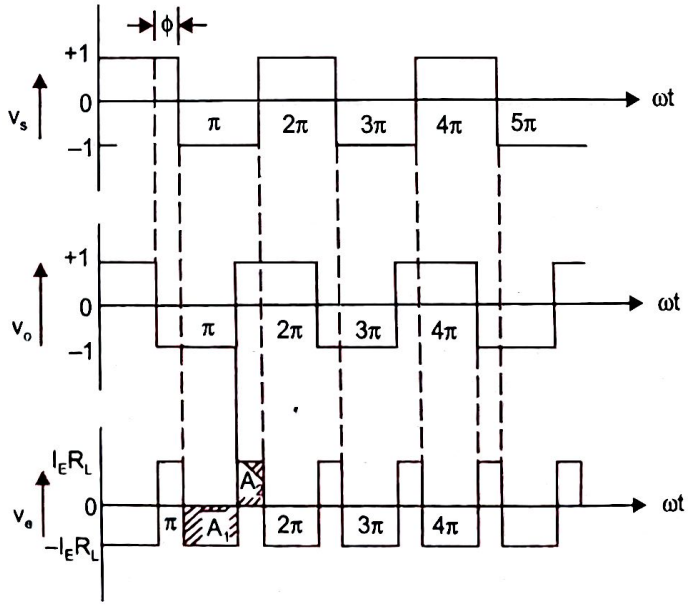


Fig. 10.4 (b) Timing diagram of input and output waveforms for balanced modulator circuit of Fig. 10.4 (a)

$$= \frac{1}{\pi}\left[I_E R_L \phi + (-I_E R_L) \times (\pi - \phi)\right] = I_E R_L \left(\frac{2\phi}{\pi} - 1\right)$$

$$= 4\frac{I_Q R_L}{\pi}\left(\phi - \frac{\pi}{2}\right) \qquad [\text{Since } I_E = 2I_Q]$$

$$= K_\phi(\phi - \pi/2) \tag{10.6}$$

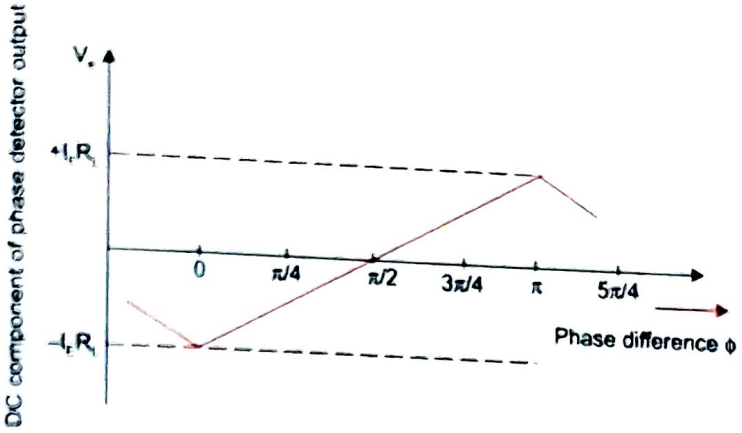


Fig. 10.4 (c) Output dc voltage versus input phase difference of balanced modulator full wave switching phase detector

where K_ϕ is the phase angle-to-voltage transfer coefficient or, the **conversion ratio of the phase detector**. This linear relationship between v_o and ϕ is depicted in Fig. 10.4 (c).

10.3.2 Digital Phase Detector

Figure 10.5 (a) shows the digital type XOR (Exclusive–OR) phase detector. It uses CMOS type 4070 Quad 2-input XOR gate. The output of the XOR gate is high when only one of the inputs signals f_s or f_o is high. This type of detector is used when both the input signals are square waves. The input and output waveforms for $f_s = f_o$ are shown in Fig. 10.5 (b). In this figure f_s is leading f_o by ϕ degrees. The variation of dc output voltage with phase difference

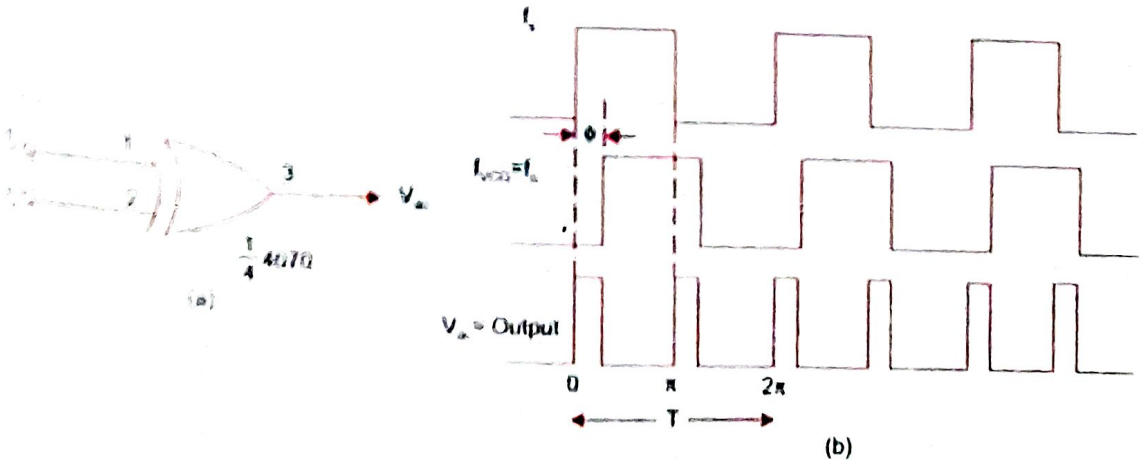


Fig. 10.5 (a) Exclusive-OR phase detector, (b) Input and output waveforms

ϕ is shown in Fig. 10.5 (c). It can be seen that the maximum dc output voltage occurs when the phase difference is π because the output of the gate remains high throughout. The slope of the curve gives the conversion ratio k_ϕ of the phase detector. So, the conversion ratio K_ϕ for a supply voltage $V_{CC} = 5$ V is,

$$K_\phi = \frac{5}{\pi} = 1.59 \text{ V/rad} \qquad (10.7)$$

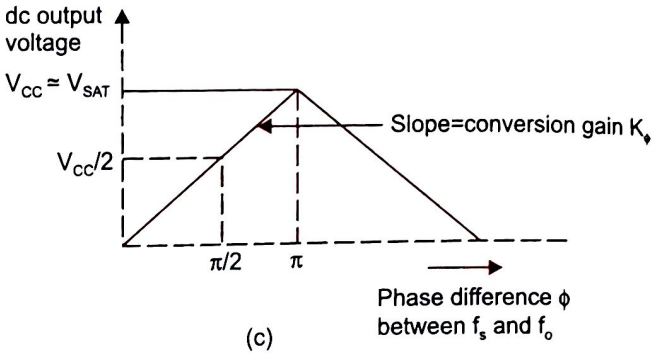


Fig. 10.5 (c) DC output voltage versus phase difference ϕ curve

Another type of digital phase detector is an ***edge-triggered phase detector*** as shown in Fig. 10.6 (a). The circuit is an R-S flip-flop made by NOR gates, such as CD 4001. This circuit is useful when f_s (incoming signal) and f_0 (VCO output) are both pulse waveforms with duty cycle less than 50 per cent. The output of the R-S flip-flop changes its state on the leading edge of f_s and f_0 as shown in Fig. 10.6 (b). The variation of dc output voltage vs phase difference between f_s and f_0 is shown in Fig. 10.6 (c). This type of detector has better capture tracking and locking characteristics as the dc output voltage is linear upto 360° compared to 180° in the case of Exclusive-OR detector.

Digital phase detector is also available in independent monolithic IC form. A typical example is MC4344/4044. This IC gives input/output transfer characteristics which is linear upto 4π radians or 720°.

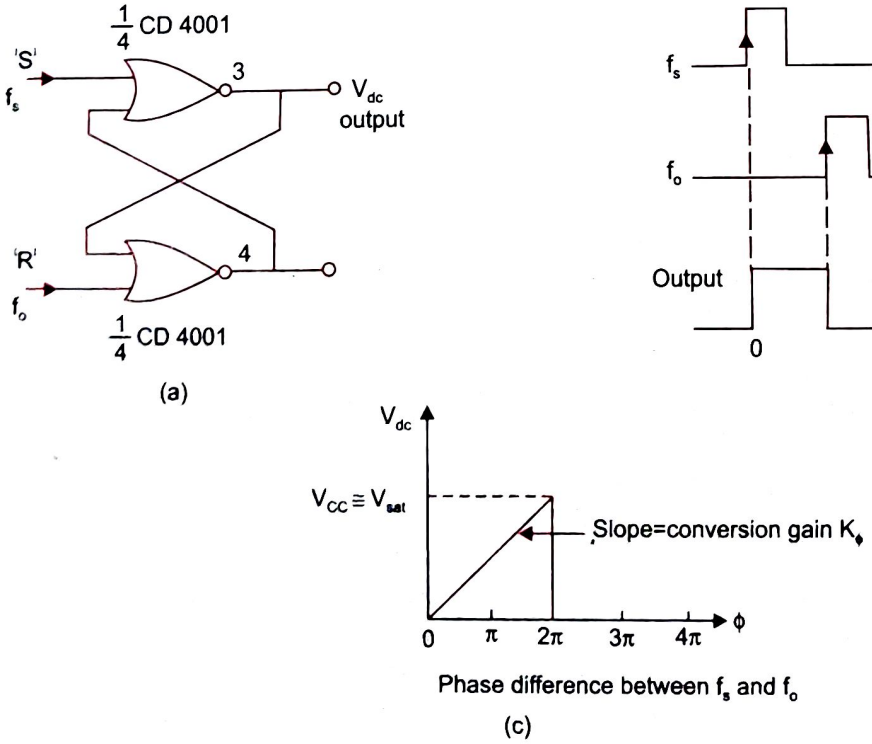


Fig. 10.6 (a) Edge-triggered phase detector using CD4001, Quad 2-input NOR gate, (b) Input and output waveforms, (c) dc output voltage vs phase difference ϕ

10.4 VOLTAGE CONTROLLED OSCILLATOR (VCO)

A common type of VCO available in IC form is Signetics NE/SE566. The pin configuration and basic block diagram of 566 VCO are shown in Fig. 10.7 (a, b). Referring to Fig. 10.7 (b), a timing capacitor C_T is linearly charged or discharged by a constant current source/sink. The amount of current can be controlled by changing the voltage v_c applied at the modulating input (pin 5) or by changing the timing resistor R_T external to IC chip. The voltage at pin 6 is held at the same voltage as pin 5. Thus, if the modulating voltage at pin 5 is increased, the voltage at pin 6 also increases, resulting in less voltage across R_T and thereby decreasing the charging current.

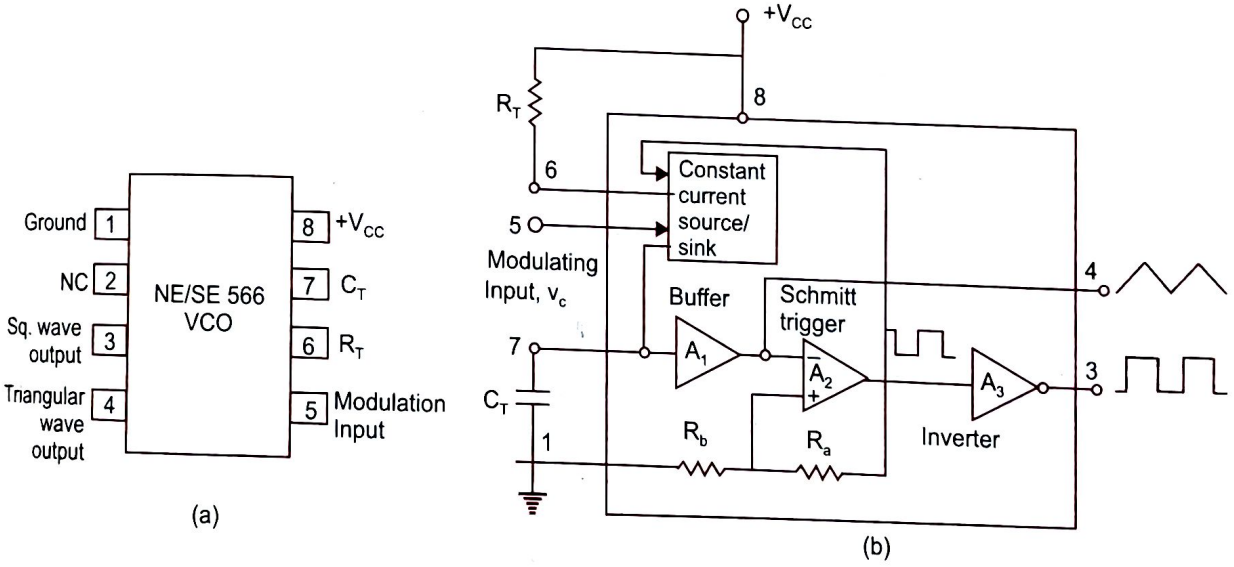


Fig. 10.7 Voltage controlled oscillator (a) Pin configuration, (b) Block diagram

A small capacitor of .001 μF should be connected between pin 5 and 6 to eliminate possible oscillations. A VCO is commonly used in converting low frequency signals such as EEGs, EKG into an audio frequency range. These audio signals can be transmitted over telephone lines or a two way radio communication systems for diagnostic purposes or can be recorded on a magnetic tape for further reference.

The voltage across the capacitor C_T is applied to the inverting input terminal of Schmitt trigger A_2 via buffer amplifier A_1. The output voltage swing of the Schmitt trigger is designed to V_{CC} and 0.5 V_{CC}. If $R_a = R_b$ in the positive feedback loop, the voltage at the non-inverting input terminal of A_2 swings from 0.5 V_{CC} to 0.25 V_{CC}. In Fig. 10.7 (c), when the voltage on the capacitor C_T exceeds 0.5 V_{CC} during charging, the output of the Schmitt trigger goes LOW (0.5 V_{CC}). The capacitor now discharges and when it is at 0.25 V_{CC}, the output of Schmitt trigger goes HIGH (V_{CC}). Since the source and sink currents are equal, capacitor charges and discharges for the same amount of time. This gives a triangular voltage waveform across C_T which is also available at pin 4. The square wave output of the Schmitt trigger is inverted* by inverter A_3 and is available at pin 3. The inverter A_3 is basically a current amplifier used to drive the load. The output waveforms are shown in Fig. 10.7 (c).

The output frequency of the VCO can be calculated as follows:

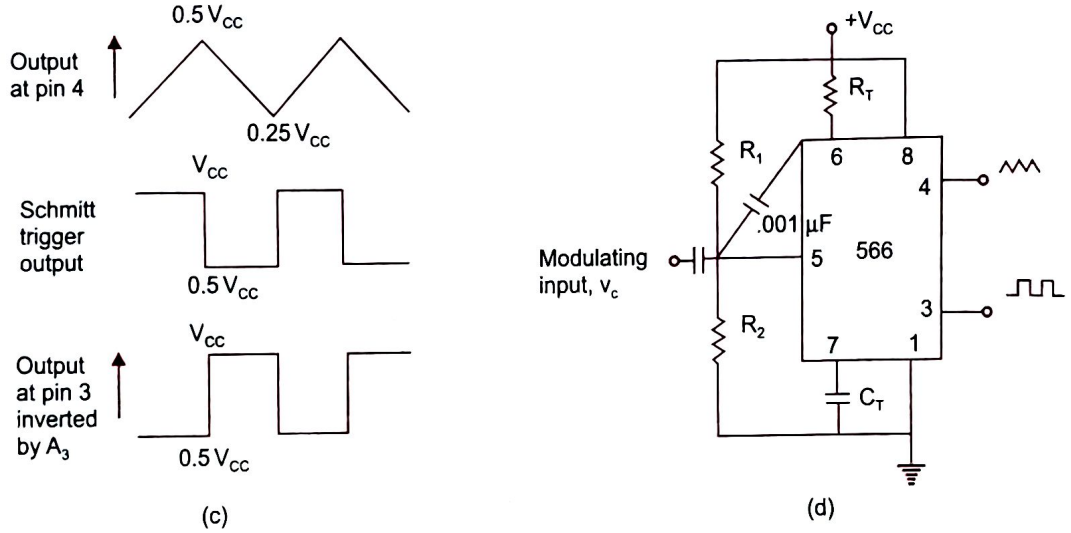


Fig. 10.7 (c) Output waveform, (d) Typical connection diagram

The total voltage on the capacitor changes from 0.25 V_{CC} to 0.5 V_{CC}. Thus $\Delta v = 0.25\ V_{CC}$. The capacitor chargers with a constant current source.

So
$$\frac{\Delta v}{\Delta t} = \frac{i}{C_T}$$

or,
$$\frac{0.25\ V_{CC}}{\Delta t} = \frac{i}{C_T}$$

or,
$$\Delta t = \frac{0.25\ V_{CC} C_T}{i} \tag{10.8}$$

The time period T of the triangular waveform = $2\Delta t$. The frequency of oscillator f_0 is,

$$f_0 = \frac{1}{T} = \frac{1}{2\,\Delta t} = \frac{i}{0.5\ V_{CC} C_T}$$

But,
$$i = \frac{V_{CC} - v_c}{R_T} \tag{10.9}$$

where, v_c is the voltage at pin 5. Therefore,

$$f_0 = \frac{2(V_{CC} - v_c)}{C_T R_T V_{CC}} \tag{10.10}$$

The output frequency of the VCO can be changed either by (i) R_T, (ii) C_T or (iii) the voltage v_c at the modulating input terminal pin 5. The voltage v_c can be varied by connecting a R_1R_2 circuit as shown in Fig. 10.7 (d). The components R_T and C_T are first selected so that VCO output frequency lies in the centre of the operating frequency range. Now the modulating input voltage is usually varied from 0.75 V_{CC} to V_{CC} which can produce a frequency variation of about 10 to 1. With no modulating input signal, if the voltage at pin 5 is biased† at (7/8) V_{CC}, Eq. (10.10) gives the VCO output frequency as,

† The expression of f_0 depends upon the initial choice of the voltage v_c. If the value of v_c is taken as 0.85 V_{CC} then f_0 comes out to be $0.3/R_TC_T$.

$$f_o = \frac{2(V_{CC} - (7/8)V_{CC})}{C_T R_T V_{CC}} = \frac{1}{4R_T C_T} = \frac{0.25}{R_T C_T} \tag{10.11}$$

Voltage to Frequency Conversion Factor

A parameter of importance for VCO is voltage to frequency conversion factor K_v and is defined as

$$K_v = \frac{\Delta f_o}{\Delta v_c}$$

Here Δv_c is the modulation voltage required to produce the frequency shift Δf_o for a VCO. If we assume that the original frequency is f_o and the new frequency is f_1, then

$$\Delta f_o = f_1 - f_o = \frac{2(V_{CC} - v_c + \Delta v_c)}{C_T R_T V_{CC}} - \frac{2(V_{CC} - v_c)}{C_T R_T V_{CC}} = \frac{2\Delta v_c}{C_T R_T V_{CC}} \tag{10.12}$$

or, $$\Delta v_c = \frac{\Delta f_o C_T R_T V_{CC}}{2} \tag{10.13}$$

Putting the value of $C_T R_T$ from Eq. (10.11)

$$\Delta v_c = \Delta f_o V_{CC}/8f_o \tag{10.14}$$

or, $$K_v = \frac{\Delta f_o}{\Delta v_c} = \frac{8 f_o}{V_{CC}} \tag{10.15}$$

Example 10.1

In a VCO, if input signal frequency f_s = 20 kHz, free running, frequency f_o = 21 kHz/V, voltage to frequency conversion factor K_V is 4 kHz/V, find the change in the dc control voltage V_c during lock.

Solution

The voltage to frequency conversion factor

$$K_v = \frac{\Delta f_o}{\Delta V_C}$$

So, $$\Delta V_C = \frac{\Delta f_o}{K_v}$$

Frequency shift $$\Delta f_o = 21 \text{ kHz} - 20 \text{ kHz}$$
$$= 1 \text{ kHz}$$

Therefore $$\Delta V = \frac{1 \times 10^3}{4 \times 10^3} V$$

$$= 0.25 \text{ V}.$$

10.5 LOW PASS FILTER

The filter used in a PLL may be either passive type as shown in Fig. 10.8 (a, b) or active type as in Fig. 10.8 (c).

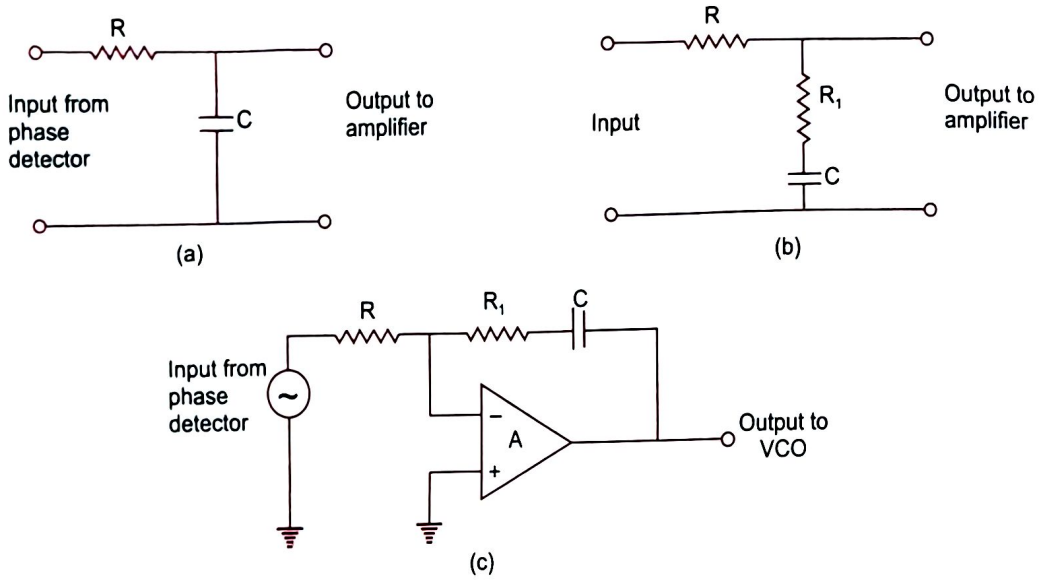


Fig. 10.8 (a) Low pass filter, (b) Passive filter, (c) Active filter

The low pass filter not only removes the high frequency components and noise, but also controls the dynamic characteristics of the PLL. These characteristics include capture and lock range, band-width and transient response. If filter band-width is reduced, the response time increases. However, reducing the band-width of the filter also reduces the capture range of the PLL. The filter serves one more important purpose. The charge on the filter capacitor gives a short time 'memory' to the PLL. Thus, even if the signal becomes less than the noise for a few cycles, the dc voltage on the capacitor continues to shift the frequency of the VCO till it picks up signal again. This produces a high noise immunity and locking stability.

Example 10.2

The free running frequency of a PLL is 300 kHz and the bandwidth of the low pass filter is 10 kHz. Will the PLL acquire lock for an input signal of 320 kHz. Also what happens if the cut-off frequency of the LPF is 25 kHz.

Solution

The phase detector outputs will be

$$f_s + f_0 = 320 \text{ kHz} + 300 \text{ kHz}$$
$$= 620 \text{ kHz}$$

and $$f_s - f_o = 320 \text{ kHz} - 300 \text{ kHz}$$
$$= 20 \text{ kHz}$$

If the bandwidth of the LPF is 10 kHz, then PLL will not lock. However, for 25 kHz BW. PLL will lock.

10.6 MONOLITHIC PHASE-LOCKED LOOP

All the different building blocks of PLL are available as independent IC packages and can be externally interconnected to make a PLL. However, a number of manufacturers have introduced monolithic PLLs too. Some of the important monolithic PLLs are SE/NE560 series introduced by Signetics and LM560 series by National Semiconductor. The SE/NE 560, 561, 562, 564, 565 and 567 mainly differ in operating frequency range, power supply requirement, frequency and bandwidth adjustment ranges. Since 565 is the most commonly used PLL, we will discuss some of the important features of this IC chip.

IC PLL 565

565 is available as a 14-pin DIP package and as 10-pin metal can package. The pin configuration and the block diagram are shown in Fig. 10.9 (a, b). The output frequency of the VCO (both inputs 2, 3 grounded) as given by Eq. (10.11) can be rewritten as,

$$f_o = \frac{0.25}{R_T C_T} \text{ Hz} \qquad (10.16)$$

where R_T and C_T are the external resistor and capacitor connected to pin 8 and pin 9. A value between 2 kΩ and 20 kΩ is recommended for R_T. The VCO free running frequency is adjusted with R_T and C_T to be at the centre of the input frequency range. It may be seen that phase locked loop is internally broken between the VCO output and the phase comparator input. A short circuit between pins 4 and 5 connects the VCO output to the phase comparator so as to compare f_o with input signal f_s. A capacitor C is connected between pin 7 and pin 10 (supply terminal) to make a low pass filter with the internal resistance of 3.6 kΩ.

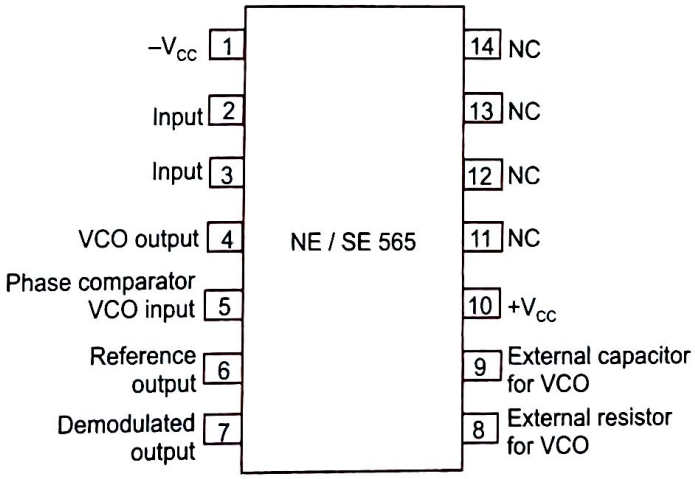


Fig. 10.9 (a) Pin diagram

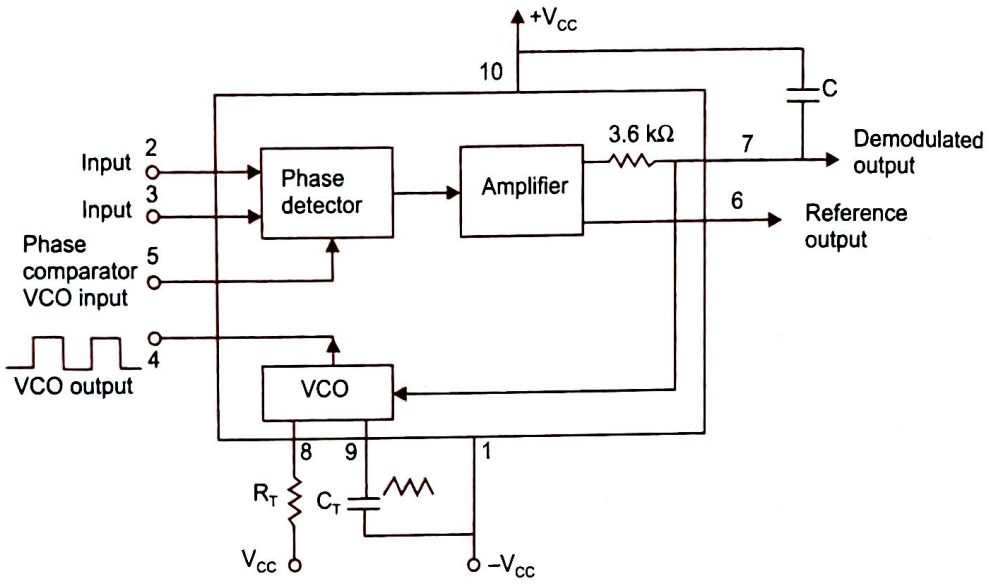


Fig. 10.9 (b) NE/SE565 PLL block diagram

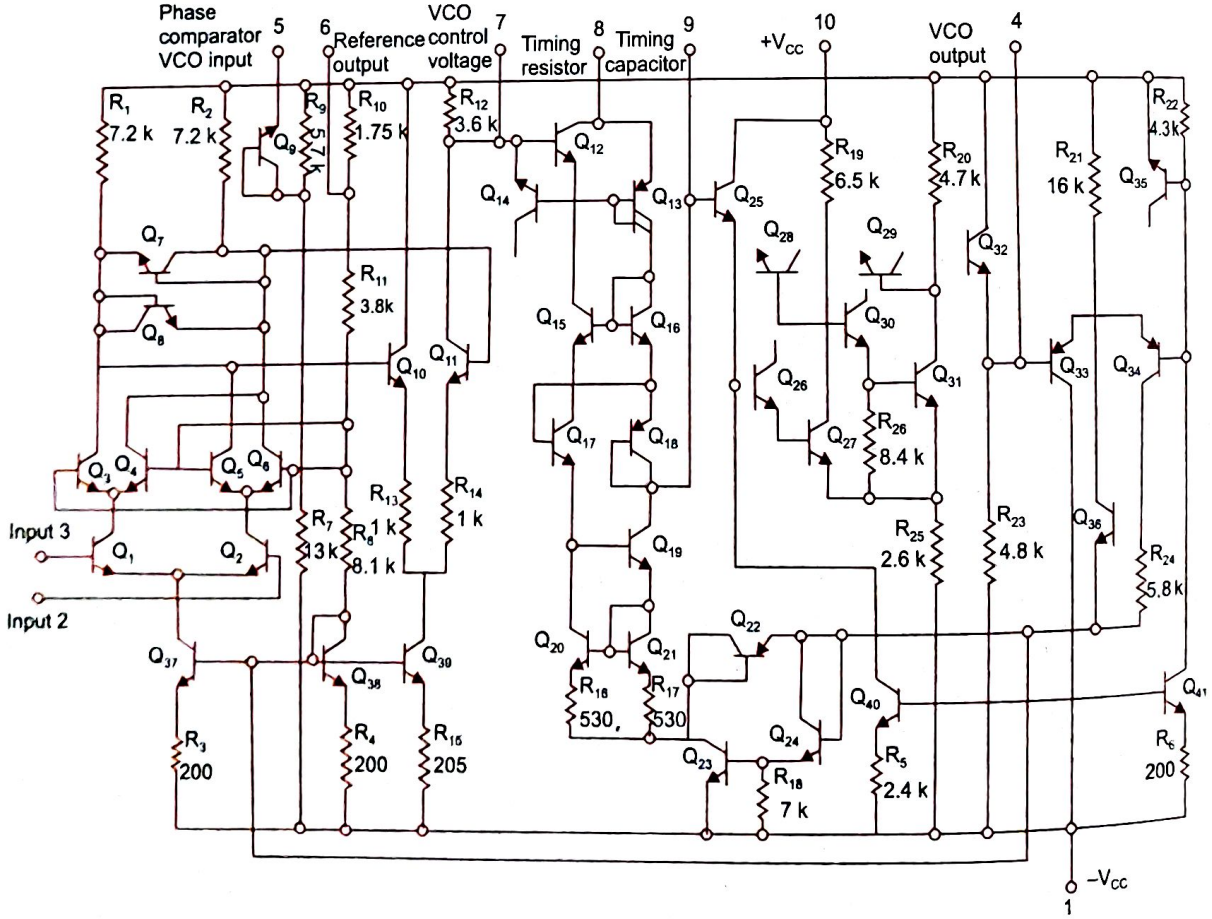


Fig. 10.10 Circuit diagram of LM565 PLL

In Fig. 10.10, a complete diagram of LM565 (National Semiconductor) IC PLL is presented. The analog phase detector is comprised of the Q_1–Q_2, Q_3–Q_4 and Q_5–Q_6 differential amplifier pairs with Q_{37} together with R_3 (200 Ω) serving as a current sink bias source. Resistors R_1 and R_2 (each 7.2 kΩ) serve as the load for the phase detector. The output voltage of the phase detector is limited by the diode-connected transistors Q_7 and Q_8 to a maximum of ±0.7 V which minimizes the effect of high amplitude noise pulses and other transient effect on the operation of the PLL. This makes the conversion ratio of the phase detector of 565 PLL as,

$$K_\phi = \frac{0.7-(-0.7)}{\pi} = \frac{1.4}{\pi} \tag{10.17}$$

A balanced output is taken from the phase detector and supplied to the Q_{10}–Q_{11} differential pair which is biased by the Q_{39} current sink. Q_{10}–Q_{11} serves as the amplifier stage (which is designed for a gain of 1.4) after phase detector. A single ended output is taken from this stage across the resistors R_{12} (3.6 kΩ). Resistor R_{12} also serves as part of the LPF when an external capacitor between pin 7 and ground of is connected.

The VCO consists of a voltage controlled current source (Q_{12} through Q_{23}). Equal charging and discharging currents are supplied to external capacitor C_T connected at pin 9. Resistor R_T is connected between pin 8 and positive supply $+V_{CC}$. The Schmitt trigger (Q_{25} through Q_{36}) with the differential amplifier output circuit (Q_{33} and Q_{34}) is part of VCO. This controls the turn-on and turn-off of Q_{23} and Q_{24} for the switching action of the current source for the charging and discharging cycles. Transistor Q_{14}, Q_{26}, Q_{30}, Q_{35} are used as diodes to obtain the desired level shift.

The important electrical parameters of 565 PLL are:

Operating frequency range	:	0.001 Hz to 500 kHz
Operating voltage range	:	±6 V to ±12 V
Input level	:	10 mV rms min. to 3 V pp max
Input impedance	:	10 kΩ typical
Output sink current	:	1 mA typical
Drift in VCO centre frequency with temperature	:	300 ppm/°C. (parts per million per degree centigrade)
Drift in VCO centre frequency with supply voltage	:	1.5 per cent/V max
Triangle wave amplitude	:	2.4 V_{pp} at ±6 V supply voltage
Square wave amplitude	:	5.4 V_{pp} at ±6 V supply voltage
Bandwidth adjustment range	:	< ±1 to ±60%

Derivation of Lock-in Range

If ϕ radians is the phase difference between the signal and the VCO voltage, then the output voltage of the analog phase detector is given by,

$$v_c = K_\phi(\phi - \pi/2) \tag{10.18}$$

where K_ϕ is the phase angle-to-voltage transfer coefficient of the phase detector. The control voltage to VCO is,

$$v_c = AK_\phi(\phi - \pi/2) \tag{10.19}$$

where A is the voltage gain of the amplifier. This v_c shifts VCO frequency from its free running frequency f_0 to a frequency f given by,

$$f = f_o + K_v v_c \tag{10.20}$$

where K_v is the voltage to frequency transfer coefficient of the VCO. When PLL is locked-in to signal frequency f_s, then we have

$$f = f_s = f_o + K_v v_c \tag{10.21}$$

since, $$v_c = (f_s - f_o)/K_v = A K_\phi (\phi - \pi/2) \tag{10.22}$$

Thus, $$\phi = \pi/2 + (f_s - f_o)/K_v K_\phi A \tag{10.23}$$

The maximum output voltage magnitude available from the phase detector occurs for $\phi = \pi$ and 0 radian (see in Fig. 10.4 (c) and $v_{e(max)} = \pm K_\phi \pi/2$ from Eq. 10.6. The corresponding value of the maximum control voltage available to drive the VCO will be,

$$v_{c(max)} = \pm (\pi/2) K_\phi A \tag{10.24}$$

The maximum VCO frequency swing that can be obtained is given by,

$$(f - f_o)_{max} = K_v v_{c(max)} = K_v K_\phi A (\pi/2) \tag{10.25}$$

Therefore, the maximum range of signal frequencies over which the PLL can remain locked will be,

$$f_s = f_o \pm (f - f_o)_{max} = f_o \pm K_v K_\phi (\pi/2) A = f_o \pm \Delta f_L \tag{10.26}$$

where $2 \Delta f_L$ will be the lock-in frequency range and is given by,

lock-in range = $$2 \Delta f_L = K_v K_\phi A \pi \tag{10.27}$$

or, $$\Delta f_L = \pm K_v K_\phi A (\pi/2) \tag{10.28}$$

The lock-in range is symmetrically located with respect to VCO free running frequency f_o. For IC PLL 565,

$$K_v = \frac{8 f_o}{V} \quad \text{(from Eq. 10.15)}$$

where $$V = +V_{CC} - (-V_{CC})$$

Again, $$K_\phi = \frac{1.4}{\pi} \quad \text{(from Eq. 10.17)}$$

and $$A = 1.4$$

Hence the lock-in range from Eq. 10.28 becomes,

$$\Delta f_L = \pm 7.8 f_o/V \tag{10.29}$$

Derivation of Capture Range

Initially, when PLL is not locked to the signal, the frequency of the VCO will be free running frequency f_o. The phase angle difference between the signal and the VCO output voltage will be,

$$\phi = (\omega_s t + \theta_s) - (\omega_o t + \theta_o) = (\omega_s - \omega_o) t + \Delta\theta \tag{10.30}$$

thus the phase angle difference does not remain constant but will change with time at a rate given by

$$\frac{d\phi}{dt} = \omega_s - \omega_o \tag{10.31}$$

The phase detector output voltage will therefore not have a dc component but will produce an ac voltage with a triangular waveform of peak amplitude $K_\phi(\pi/2)$ and a fundamental frequency $(f_s - f_o) = \Delta f$.

The low pass filter (LPF) is a simple RC network having transfer function

$$T(jf) = \frac{1}{1 + j(f/f_1)} \tag{10.32}$$

where $f_1 = 1/2\,\pi\,RC$ is the 3-dB point of LPF. In the slope portion of LPF where $(f/f_1)^2 >> 1$, then

$$T(f) \simeq \frac{f_1}{jf} \tag{10.33}$$

The fundamental frequency term supplied to the LPF by the phase detector will be the difference frequency $\Delta f = f_s - f_o$. If $\Delta f > 3f_1$, the LPF transfer function will be approximately,

$$T(\Delta f) \simeq f_1/\Delta f = f_1/(f_s - f_o) \tag{10.34}$$

The voltage v_c to drive the VCO is,

$$v_c = v_e \times T(f) \times A \tag{10.35}$$

or,
$$v_{c(max)} = v_{e(max)} \times T(f) \times A$$
$$= \pm K_\phi (\pi/2) A\,(f_1/\Delta f). \text{ (from Eq. (10.24))} \tag{10.36}$$

Then the corresponding value of the maximum VCO frequency shift is,

$$(f - f_o)_{max} = K_v\, v_{c(max)} = \pm K_v K_\phi (\pi/2) A\,(f_1/\Delta f) \tag{10.37}$$

For the acquisition of signal frequency, we should put $f = f_s$, so that the maximum signal frequency range that can be acquired by PLL is,

$$(f_s - f_o)_{max} = \pm K_v K_\phi (\pi/2) A\,(f_1/\Delta f_c) \tag{10.38}$$

Now
$$\Delta f_c = (f_s - f_o)_{max}$$

so,
$$(\Delta f_c)^2 = K_v K_\phi (\pi/2) A f_1 \text{ (from Eq. (10.38))}$$

since,
$$\Delta f_L = \pm K_v K_\phi (\pi/2) A$$

we get,
$$(\Delta f_c) \simeq \pm\sqrt{f_1\, \Delta f_L} \tag{10.39}$$

Therefore, the total capture range is,

$$2\,\Delta f_c \simeq 2\sqrt{f_1\, \Delta f_L} \tag{10.40}$$

where the lock-in range $= 2\,\Delta f_L = K_v\, K_\phi\, A\,\pi$. In case of IC PLL 565, $R = 3.6$ kΩ, so the capture range is

$$\pm\left[\frac{\Delta f_L}{2\pi(3.6 \times 10^3)\,C}\right]^{\frac{1}{2}} \tag{10.41}$$

where C is in farads.

The capture range is symmetrically located with respect to VCO free running frequency f_o as is shown in Fig. 10.11. The PLL cannot acquire a signal outside the capture range, but

once captured, it will hold on till the signal frequency goes beyond the lock-in range. In order to increase the ability of lock-in range, large capture range is required. However, a large capture range will make the PLL more susceptible to noise and undesirable signal. Hence a suitable compromise is often reached between these two opposing requirements of the

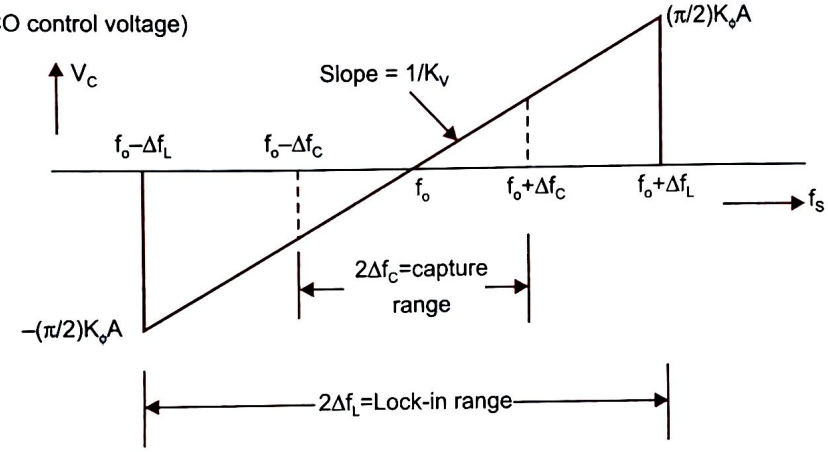


Fig. 10.11 PLL lock-in range and capture range

capture range. Many a times the LPF band-width is first set for a large value for initial acquisition of signal, then once the signal is captured, the band-width of LPF is reduced substantially. This will minimize the interference of undesirable signals and noise.

Example 10.3

The free running frequency of a 565 PLL is 100 kHz, the filter capacitar is 2μF and supply voltage is ± 6V. Compute the lock-in-range, capture range frequency and the value of external components R_T & C_T.

Solution

Given f_o = 100 kHz, C = 2μF and V_{CC} = ± 6V.

We know that the lock-in range is given by

$$\Delta f_L = \pm \frac{7.8 f_o}{V} \qquad \text{[from Eq. (10.29)]}$$

$$= \pm \frac{7.8 f_o}{V_{CC} - (-V_{CC})}$$

$$= \pm \frac{7.8 \times 100}{6 - (-6)V} = \pm 65 \text{ kHz}$$

Thus lock-in range = ± 65 kHz

The capture range, $2\Delta f_C$ is given by

$$2\Delta f_C = \pm \sqrt{\frac{\Delta f_L}{2\pi(\times 3.6 \times 10^3)C}} \qquad \text{[from Eq. (10.41)]}$$

Putting the values and solving, we get

$$2\Delta f_C = 2.397 \text{ kHz}$$

Further, the free running frequency, f_o is

$$f_o = \frac{0.25}{R_T C_T} \qquad \text{[from Eq. (10.16)]}$$

Assuming $R_T = 10\text{K}\Omega$, we obtain

$C_T = 250$ pF.

Example 10.4

Compute the free running frequency f_o, lock-in range and capture range of PLL 565. Assume $R_T = 20$ KΩ, $C_T = 0.01$ μF, $C = 1$ μF and supply voltage is ± 6V.

Solution

Given $R_T = 10$ KΩ, $C_T = 0.01$ μF and $C = 1\mu$F

The free running frequency of VCO is

$$f_o = \frac{0.25}{R_T C_T} = \frac{0.25}{10 \times 10^3 \times 0.01 \times 10^{-6}}$$

$$= 2.5 \text{ kHz}$$

The lock in range is given by

$$\Delta f_L = \pm \frac{7.8 f_o}{V} = \pm \frac{7.8 \times 2.5 \times 10^3}{12}$$

$$= 1.62 \text{ kHz}$$

The capture range is given by

$$2\Delta f_C = \sqrt{\frac{\Delta f_L}{2\pi \times (3.6 \times 10^3) C}}$$

$$= \sqrt{\frac{2 \times 1.62 \times 10^3}{2\pi \times (3.6 \times 10^3) \times 1 \times 10^{-6}}}$$

$$= 378 \text{ Hz}$$

10.7 PLL APPLICATIONS

The output from a PLL system can be obtained either as the voltage signal $v_c(t)$ corresponding to the error voltage in the feedback loop, or as a frequency signal at VCO output terminal. The voltage output is used in frequency discriminator application whereas the frequency output is used in signal conditioning, frequency synthesis or clock recovery applications.

Consider the case of voltage output. When PLL is locked to an input frequency, the error voltage $v_c(t)$ is proportional to $(f_s - f_o)$. If the input frequency is varied as in the case of FM signal, v_c will also vary in order to maintain the lock. Thus the voltage output serves as a frequency discriminator which converts the input frequency changes to voltage changes.

In the case of frequency output, if the input signal is comprised of many frequency components corrupted with noise and other disturbances, the PLL can be made to lock, selectively on one particular frequency component at the input. The output of VCO would then regenerate that particular frequency (because of LPF which gives output for beat frequency) and attenuate heavily other frequencies. VCO output thus can be used for regenerating or reconditioning a desired frequency signal (which is weak and buried in noise) out of many undesirable frequency signals.

Some of the typical applications of PLL are discussed now.

10.7.1 Frequency Multiplication/Division

Figure 10.12 gives the block diagram of a ***frequency multiplier*** using PLL. A divide by N network is inserted between the VCO output and the phase comparator input. In the locked state, the VCO output frequency f_0 is given by,

$$f_0 = N f_s \tag{10.42}$$

The multiplication factor can be obtained by selecting a proper scaling factor N of the counter.

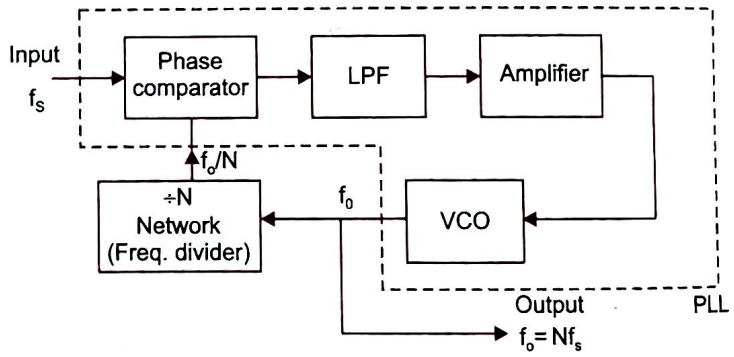


Fig. 10.12 Frequency multiplier using IC PLL

Frequency multiplication can also be obtained by using PLL in its harmonic locking mode. If the input signal is rich in harmonics e.g. square wave, pulse train etc., then VCO can be directly locked to the n-th harmonic of the input signal without connecting any frequency divider in between. However, as the amplitude of the higher order harmonics becomes less, effective locking may not take place for high values of n. Typically n is kept less than 10.

The circuit of Fig. 10.12 can also be used for frequency division. Since the VCO output (a square wave) is rich in harmonics, it is possible to lock the m-th harmonic of the VCO output with the input signal f_s. The output f_0 of VCO is now given by

$$f_0 = \frac{f_s}{m} \tag{10.43}$$

10.7.2 Frequency Translation

A schematic for shifting the frequency of an oscillator by a small factor is shown in Fig. 10.13. It can be seen that a mixer (or multiplier) and a low pass filter are connected externally to the PLL. The signal f_s which has to be shifted and the output frequency f_0 of the VCO are applied as inputs to the mixer. The output of the mixer contains the sum and difference of f_s and f_0. However, the output of LPF contains only the difference signal $(f_0 - f_s)$. The translation or offset frequency $f_1 (f_1 << f_s)$ is applied to the phase comparator. When PLL is in locked state,

$$f_0 - f_s = f_1$$

or

$$f_0 = f_s + f_1 \tag{10.44}$$

Thus, it is possible to shift the incoming frequency f_s by f_1.

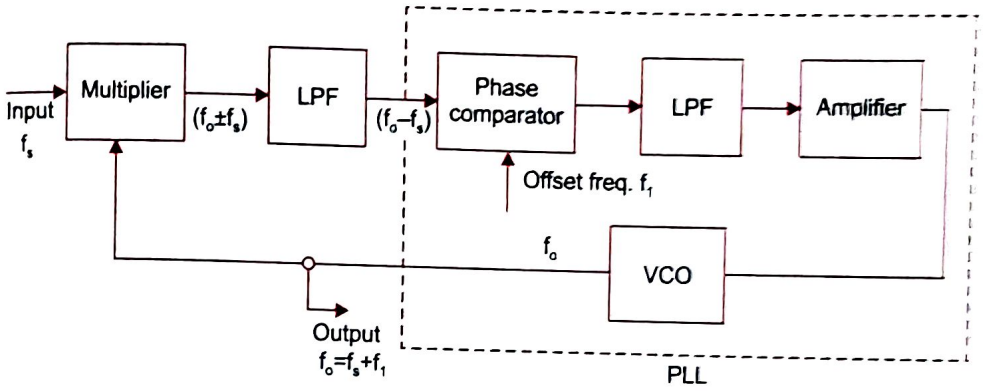


Fig. 10.13 PLL used as a frequency translator

10.7.3 AM Detection

A PLL may be used to demodulate AM signals as shown in Fig. 10.14. The PLL is locked to the carrier frequency of the incoming AM signal. The output of VCO which has the same frequency as the carrier, but unmodulated is fed to the multiplier. Since VCO output is always 90° out of phase with the incoming AM signal under the locked condition, the AM input signal is also shifted in phase by 90° before being fed to the multiplier. This makes both the signals applied to the multiplier in same phase. The output of the multiplier contains both the sum and the difference signals, the demodulated output is obtained after filtering high frequency components by the LPF. Since the PLL responds only to the carrier frequencies which are very close to the VCO output, a PLL AM detector exhibits a high degree of selectivity and noise immunity which is not possible with conventional peak detector type AM modulators.

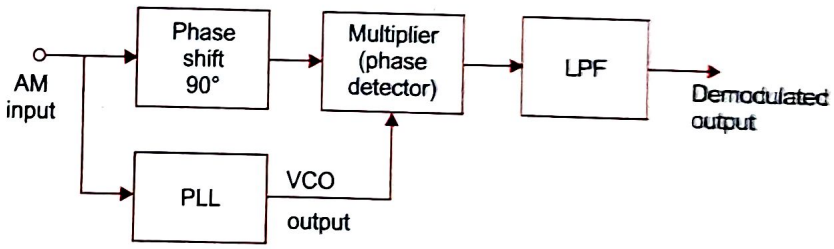


Fig. 10.14 PLL used as AM demodulator

10.7.4 FM Demodulation

If PLL is locked to a FM signal, the VCO tracks the instantaneous frequency of the input signal. The filtered error voltage which controls the VCO and maintains lock with the input signal is the demodulated FM output. The VCO transfer characteristics determine the linearity of the demodulated output. Since, VCO used in IC PLL is highly linear, it is possible to realize highly linear FM demodulators.

10.7.5 Frequency Shift Keying (FSK) Demodulator

In digital data communication and computer peripheral, binary data is transmitted by means of a carrier frequency which is shifted between two preset frequencies. This type of data transmission is called frequency shift keying (FSK) technique. The binary data can be retrieved

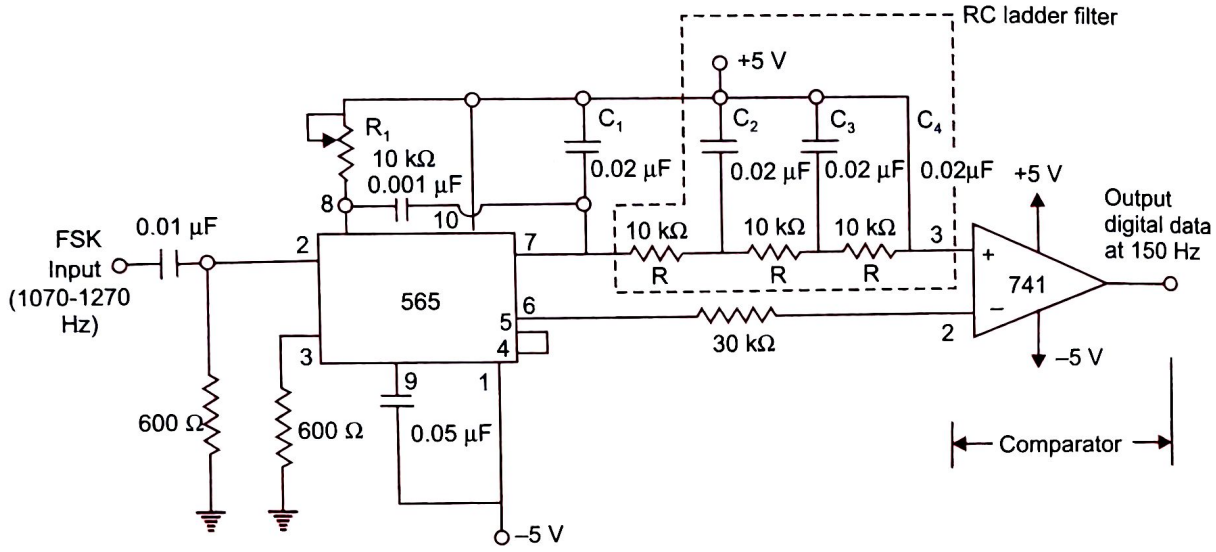


Fig. 10.15 FSK demodulator

using a FSK demodulator at the receiving end. The 565 PLL is very useful as a FSK demodulator. Figure 10.15 shows FSK demodulator using PLL for tele-typewriter signals of 1070 Hz and 1270 Hz. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output. A three stage filter removes the carrier component and the output signal is made logic compatible by a voltage comparator.

SUMMARY

1. A phase locked loop consists of a phase detector, low pass filter, amplifier and a VCO in feedback loop.
2. The important characteristics of a PLL are: lock-in range, capture range and pull-in-time.
3. The lock-in range is usually greater than the capture range. The capture range depends upon the LPF characteristics.
4. The phase detectors are of two types: analog and digital. The phase detector is basically a multiplier.
5. The frequency of VCO can be set by an external capacitor and resistor. The output frequency f_0 of VCO is compared with the incoming signal f_s. When $f_0 = f_s$, the PLL is said to be locked.
6. The low pass filter may be passive or active type. The LPF controls the capture range and lock range of PLL.
7. Signetics SE/NE 560 series – 560, 561, 562, 564, 565 and 567 are monolithic PLLs. All the blocks of a PLL are also available as independent ICs and can be interconnected to make a PLL.
8. The PLLs are used as frequency multiplier, divider, AM and FM demodulator, FSK demodulator etc.

REVIEW QUESTIONS

10.1. List the basic building blocks of a PLL.
10.2. Define capture range, lock-in range and pull-in-time.
10.3. Which is greater 'Capture range' or 'Lock-in range'?

10.4. What is the major difference between digital and analog PLLs?
10.5. Give the block diagram of IC 566 VCO and explain its operation.
10.6. What is the range of modulating input voltage applied to a VCO?
10.7. List the applications of PLL.
10.8. Draw the circuit of a PLL AM detector and explain its operation.

PROBLEMS

10.1. In the VCO of Fig. 10.7 calculate the change in output frequency if the supply voltage is varied between 9 V and 11 V. Assume V_{cc} = 12 V, R_T = 6.8 kΩ, C_T = 75 pF, R_1 = 15 kΩ and R_2 = 100 kΩ.
10.2. Determine the dc control voltage v_c at lock if signal frequency f_s = 10 kHz, VCO free running frequency is 10.66 kHz and the voltage to frequency transfer coefficient of VCO is 6600 Hz/V.
10.3. If f_s = 100 kHz, the voltage to frequency transfer coefficient of VCO, K_v = 2 MHz/V, f_0 the VCO frequency is 5 MHz and N = 100 in the frequency multiplier of Fig. 10.12, what is the dc control voltage at lock?
10.4. Calculate output frequency f_0, lock range Δf_L and capture range Δf_c of a 565 PLL if R_T = 10 kΩ, C_T = 0.01 μF and C = 10 μF.
10.5. Repeat Problem 10.4 for C_T = 470 pF.

EXPERIMENT

(a) To study the operation of NE 565 PLL.
(b) To use NE 565 as a multiplier.

PROCEDURE

1. Make connections of the PLL as shown in Fig. E. 10.1 (a).
2. Measure the free running frequency of VCO at pin 4, with the input signal V_{in} set equal to zero. Compare it with the calculated value = $0.25/R_TC_T$.
3. Now apply the input signal of 1 V_{pp} square wave at a 1 kHz to pin 2. Connect one channel of the scope to pin 2 and display this signal on the scope.

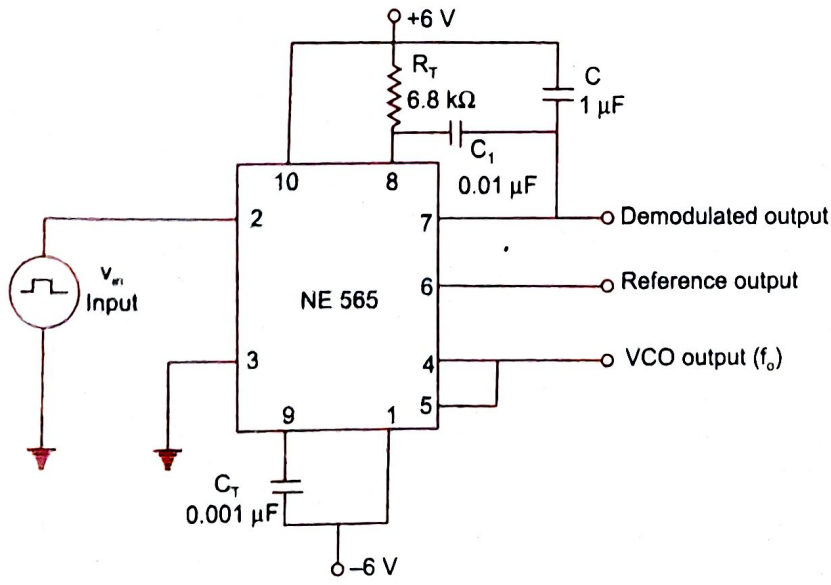


Fig. E. 10.1 (a) NE565 PLL connection diagram

4. Gradually increase the input frequency till the PLL is locked to the input frequency. This frequency f_1 gives the lower end of the capture range. Go on increasing the input frequency, till PLL tracks the input signal, say, to a frequency f_2. This frequency f_2 gives the upper end of the lock range. If input frequency is increased further, the loop will get unlocked.
5. Now gradually decrease the input frequency till the PLL is again locked. This is the frequency f_3, the upper end of the capture range. Keep on decreasing the input frequency until the loop is unlocked. This frequency f_4 gives the lower end of the lock range.
6. The lock-in range $\Delta f_L = (f_2 - f_4)$. Compare it with the calculated value of $\frac{\pm 7.8 f_o}{12}$. Also the capture range is $\Delta f_c = (f_3 - f_1)$. Compare it with the calculated value of capture range.

$$\Delta f_c = \pm \left[\frac{\Delta f_L}{(2\pi)(3.6)(10^3) \times C} \right]^{\frac{1}{2}}$$

7. To use PLL as a multiplier, make connections as shown in Fig. E. 10.1 (b). The circuit uses a 4-bit binary counter 7490 used as a divide-by-5 circuit.

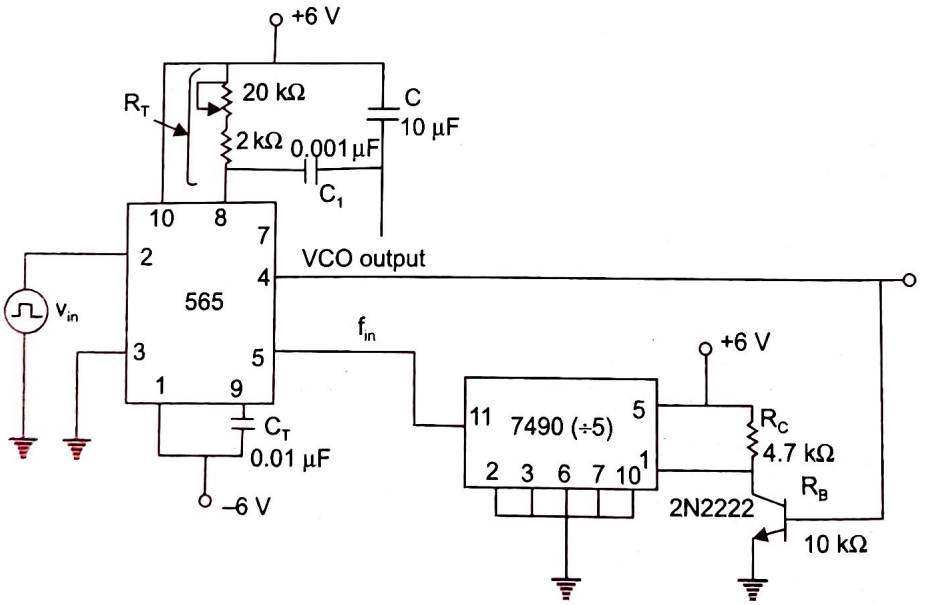


Fig. E. 10.1 (b) NE 565 as a frequency multiplier

8. Set the input signal at 1 V_{pp} square wave at 500 Hz.
9. Vary the VCO frequency by adjusting the 20 kΩ potentiometer till the PLL is locked. Measure the output frequency. It should be 5 times the input frequency.
10. Repeat steps 8, 9 for input frequency of 1 kHz and 1.5 kHz.

6

VOLTAGE REGULATOR

6.1 INTRODUCTION

The function of a voltage regulator is to provide a stable dc voltage for powering other electronic circuits. A voltage regulator should be capable of providing substantial output current. Voltage regulators are classified as:

Series regulator
Switching regulator

Series regulators use a power transistor connected in series between the unregulated dc input and the load. The output voltage is controlled by the continuous voltage drop taking place across the series pass transistor. Since the transistor conducts in the active or linear region, these regulators are also called linear regulators. Linear regulators may have fixed or variable output voltage and could be positive or negative. The schematic, important characteristics, data sheet, short circuit protection, current fold-back, current boosting techniques for linear voltage regulators such as 78 XX, 79 XX series, 723 IC are discussed.

Switching regulators, on the other hand, operate the power transistor as a high frequency *on/off* switch, so that the power transistor does not conduct current continuously. This gives improved efficiency over series regulator. In Sec. 6.4, the principle of switching power supply and its advantages over linear type of voltage regulator are discussed.

6.2 SERIES OP-AMP REGULATOR

A voltage regulator is an electronic circuit that provides a stable dc voltage independent of the load current, temperature and ac line voltage variations. Figure 6.1 shows a regulated power supply using discrete components. The circuit consists of following four parts:

1. Reference voltage circuit
2. Error amplifier
3. Series pass transistor
4. Feedback network.

It can be seen from Fig. 6.1 that the power transistor Q_1 is in series with the unregulated dc voltage V_{in} and the regulated output voltage V_o. So it must absorb the difference between these two voltages whenever any fluctuation in output voltage V_o occurs. The transistor Q_1

is also connected as an emitter follower and therefore provides sufficient current gain to drive the load. The output voltage is sampled by the $R_1 - R_2$ divider and fed back to the (–) input terminal of the op-amp error amplifier. This sampled voltage is compared with the reference voltage V_{ref} (usually obtained by a zener diode). The output V_o' of the error amplifier drives the series transistor Q_1.

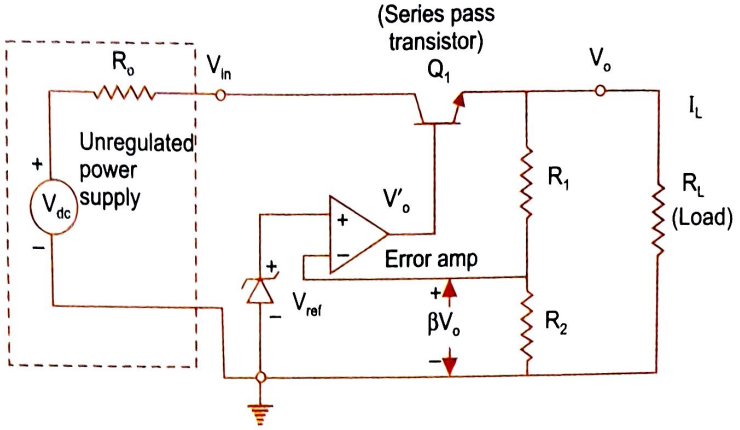


Fig. 6.1 A regulated power supply

If the output voltage increases, say, due to variation in load current, the sampled voltage βV_0 also increases where

$$\beta = \frac{R_2}{R_1 + R_2} \tag{6.1}$$

This, in turn, reduces the output voltage V_0' of the diff-amp due to the 180° phase difference provided by the op-amp amplifier. V_0' is applied to the base of Q_1, which is used as an emitter follower. So V_0 follows V_0', that is V_0 also reduces. Hence the increase in V_0 is nullified. Similarly, reduction in output voltage also gets regulated.

6.3 IC VOLTAGE REGULATORS

With the advent of micro-electronics, it is possible to incorporate the complete circuit of Fig. 6.1 on a monolithic silicon chip. This gives low cost, high reliability, reduction in size and excellent performance. Examples of monolithic regulators are 78 XX/79 XX series and 723 general purpose regulators.

6.3.1 Fixed Voltage Series Regulator

78 XX series are three terminal, positive fixed voltage regulators. There are seven output voltage options available such as 5, 6, 8, 12, 15, 18 and 24 V. In 78 XX, the last two numbers (XX) indicate the output voltage. Thus 7815 represents a 15 V regulator. There are also available 79 XX series of fixed output, negative voltage regulators which are complements to the 78 XX series devices. There are two extra voltage options of – 2 V and – 5.2 V available in 79 XX series. These regulators are available in two types of packages.

Metal package (TO – 3 type)
Plastic package (TO – 220 type)

Figure 6.2 shows the standard representation of monolithic voltage regulator. A capacitor C_i (0.33 μF) is usually connected between input terminal and ground to cancel the inductive effects due to long distribution leads. The output capacitor C_0 (1 μF) improves the transient response.

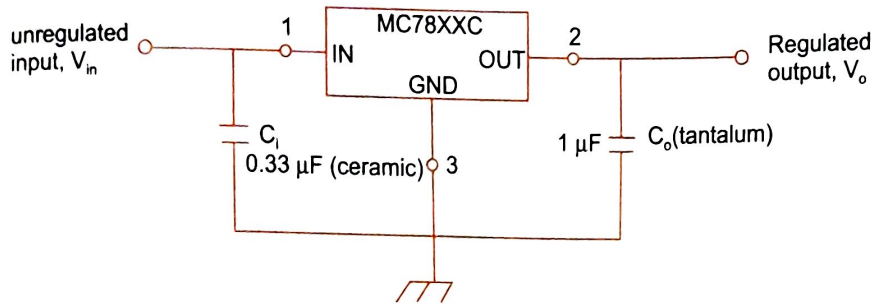


Fig. 6.2 Standard representation of a three terminal positive monolithic regulator

National Semiconductor also produces three terminal voltage regulators in LM series. There are three series available for different operating temperature ranges:

LM	100	series	−55°C	to	+125°C
LM	200	series	−25°C	to	+85°C
LM	300	series	0°C	to	+70°C

The popular series are LM 340 positive regulators and LM 320 negative regulators with output ratings comparable to 78 XX/79 XX series.

Characteristics

There are four characteristics of three terminal IC regulators which must be mentioned.

1. V_o : The regulated output voltage is fixed at a value as specified by the manufacturer. There are a number of models available for different output voltages, for example, 78 XX series has output voltage at 5, 6, 8 etc.
2. $|V_{in}| \geq |V_o| + 2$ volts: The unregulated input voltage must be atleast 2 V more than the regulated output voltage. For example, if $V_o = 5$ V, then $V_{in} = 7$ V.
3. $I_{o\,(max)}$: The load current may vary from 0 to rated maximum output current. The IC is usually provided with a heat sink, otherwise it may not provide the rated maximum output current.
4. Thermal shutdown: The IC has a temperature sensor (built-in) which turns off the IC when it becomes too hot (usually 125° C to 150°C). The output current will drop and remains there until the IC has cooled significantly.

Table 6.1 gives the electrical characteristics of 7805 voltage regulator and the connection diagram of packages available. Some of the important performance parameters listed in the data sheet are explained as follows:

Line/Input Regulation

It is defined as the percentage change in the output voltage for a change in the input voltage. It is usually expressed in millivolts or as a percentage of the output voltage. Typical value of line regulation from the data sheet of 7805 is 3 mV.

Table 6.1 Electrical characteristics of 7805 voltage regulator

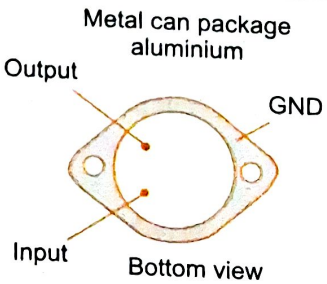
Absolute Maximum Ratings

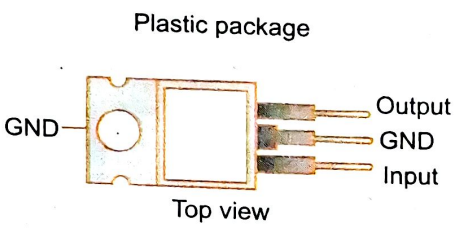
Input Voltage (5 V through 18 V)	35 V
(24 V)	40 V
Internal Power Dissipation	Internally limited
Storage Temperature Range	–65°C to +150°C
Operating Junction Temperature Range	
µA7800	–55°C to +150°C
µA7800C	0°C to +125°C

7805C

Electrical Characteristics V_{IN} = 10 V, I_{OUT} = 500 mA, 0°C ≤ T_j ≤ 125°C, C_{IN} = 0.33 µF, C_{OUT} = 0.1 µF, unless otherwise specified.

Characteristic	*Condition*	*Min*	*Typ*	*Max*	*Unit*
Output Voltage	T_j = 25°C	4.8	5.0	5.2	V
Line Regulation	T_j = 25°C, 7 V ≤ V_{IN} ≤ V		3	100	mV
	8 V ≤ V_{IN} ≤ 12 V		1	50	mV
Load Regulation	T_j = 25°C, 5 mA ≤ I_{OUT} ≤ 1.5 A		15	100	mV
	250 mA ≤ I_{OUT} ≤ 750 mA		5	50	mV
Output Voltage	7 V ≤ V_{IN} ≤ 20 V, 5 mA ≤ I_{OUT} ≤ 1.0 A, P ≤ 15 W	4.75		5.25	V
Quiescent Current	T_j = 25°C		4.2	8.0	mA
Quiescent Current with line	7 V ≤ V_{IN} ≤ 25 V			1.3	mA
Change with load	5 mA ≤ I_{OUT} ≤ 1.0 A			0.5	mA
Output Noise Voltage	T_A = 25°C, 10 Hz ≤ 1 ≤ 100 kHz		40		µV
Ripple Rejection	f = 120 Hz, 8 V ≤ V_{IN} ≤ 18 V	62	78		dB
Dropout Voltage	I_{OUT} = 1.0 A, T_j = 25°C		2.0		V
Output Resistance	f = 1 kHz		17		mΩ
Short-Circuit Current	T_j = 25°C. V_{IN} = 35 V		750		mA
Peak Output Current	T_j = 25°C		2.2		A
Average Temperature Coefficient of Output Voltage	I_{OUT} = 5 mA, 0°C ≤ T_j ≤ 125°C		1.1		mV/°C





Load Regulation

It is defined as the change in output voltage for a change in load current and is also expressed in millivolts or as a percentage of V_o. Typical value of load regulation for 7805 is 15 mV for 5 mA < I_o < 1.5 A.

Ripple Rejection

The IC regulator not only keeps the output voltage constant but also reduces the amount of ripple voltage. It is usually expressed in dB. Typical value for 7805 is 78 dB.

The Schematic diagram of MC 78 XXC* is shown in Fig. 6.3. The circuit consists of a reference voltage V_{ref}. This circuit basically consists of level shifter with zener diode input and the transistor Q_9 used as emitter follower buffer. The circuit enclosed in the shaded region is a difference amplifier consisting of a current mirror (Q_4, Q_5), and an active load (Q_6, Q_7, Q_8). The combination of R_1R_2 forms the feedback network for sampling the output voltage. The sampled voltage is fed to one of the inputs of the difference amplifier. The Darlington pair Q' Q'' forms series pass element Q_1 of the circuit shown in Fig. 6.1.

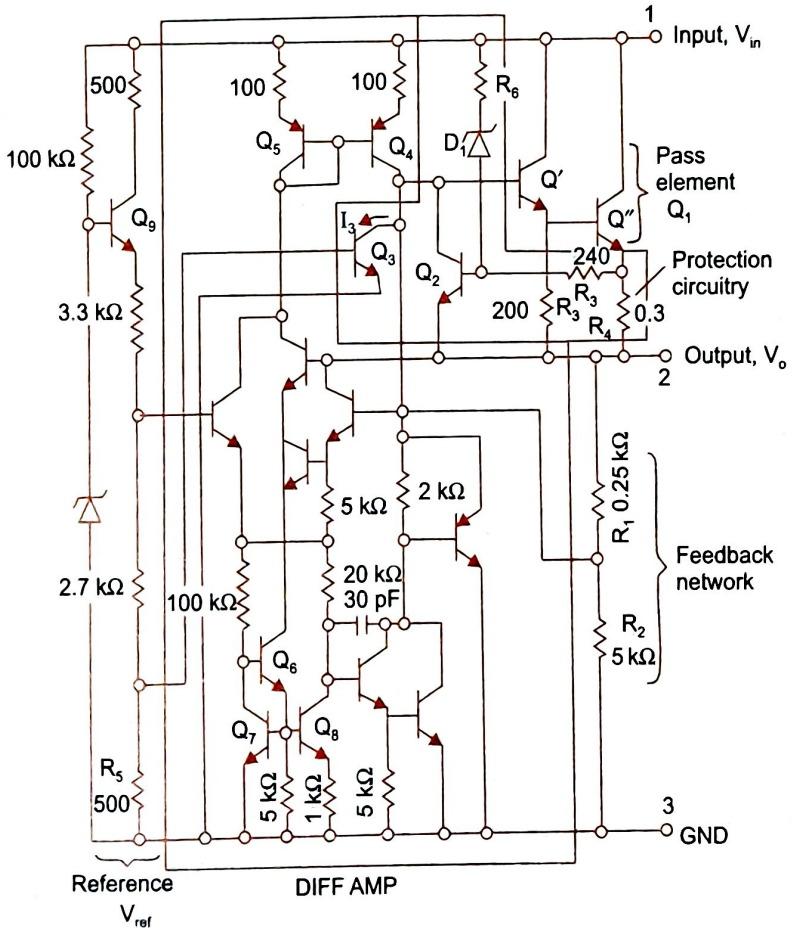


Fig. 6.3 Schematic diagram for MC 7800C series monolithic regulator

*C stands for commercial use.

The monolithic regulator has in-built circuitry enclosed in the solid line to provide:

Over-current protection.

Thermal overload protection.

Current is limited by R_3, R_4 and transistor Q_2. If the output voltage goes low due to overload, the excess voltage appears across the pass element (Q'-Q''), that is, across the collector emitter of Q''. When this voltage is more than the break-down voltage of the zener diode D_1, it starts conducting. This provides sufficient base current to transistor Q_2 and drives it ***on***. Now, because of the collector current of Q_2 when fully ***on***, current flowing to the base of Q' is reduced. This in turn reduces the conduction of Q''. Thus the volt-ampere product of the pass element (Q'-Q'') is limited.

The thermal overload protection is provided by the resistor R_5 and transistor Q_3. The voltage drop across resistor R_5 is directly applied to the base-emitter of Q_3. When the temperature goes high, Q_3 conducts more, thereby reducing the base drive of $Q'Q''$ combination. This provides thermal protection.

Current Source

The three terminal fixed voltage regulator can be used as a current source. Figure 6.4 (a) shows the circuit where 7805 has been wired to supply a current of 1 ampere to a 10 Ω, 10 watt load.

$$I_L = I_R + I_Q \tag{6.2}$$

where I_Q is the quiescent current and is about 4.2 mA for 7805. (See Table 6.1)

$$I_L = \frac{V_R}{R} + I_Q \tag{6.3}$$

Since $I_L = 1$ A, $$\frac{V_R}{R} \simeq 1 \text{ A } (I_Q << I_L) \tag{6.4}$$

Also $V_R = 5$ V (Voltage between terminal 2 and 3)

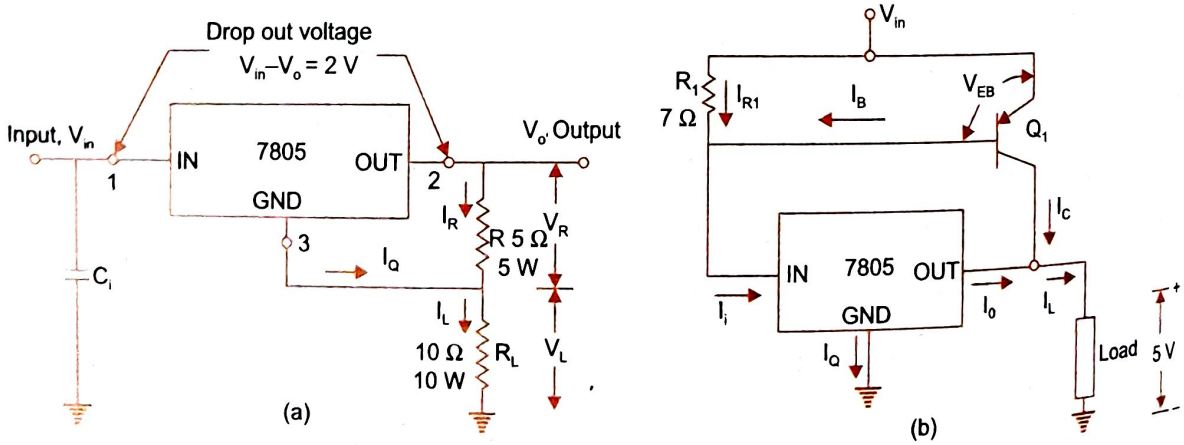


Fig. 6.4 (a) IC 7805 as a current source (b) Boosting a three terminal regulator

So the value of R required is (6.5)

$$R = 5 \text{ V}/1 \text{ A} = 5 \Omega$$

Thus choose $R = 5 \Omega$ to deliver 1 A current to a load of 10 Ω.

Boosting IC Regulator Output Current

It is possible to boost the output current of a three terminal regulator simply by connecting an external pass transistor in parallel with the regulator as shown in Fig. 6.4 (b).

Let us now see how the circuit works. For low load currents, the voltage drop across R_1 is insufficient (<0.7 V) to turn on transistor Q_1 and the regulator itself is able to supply the load current. However, as I_L increases, the voltage drop across R_1 increases. When this voltage drop is approximately 0.7 V, the transistor Q_1 turns on. It can be easily seen that if I_L = 100 mA, the voltage drop across R_1 is equal to 7 Ω × 100 mA = 0.7 V. Thus, if I_L increases more than 100 mA, the transistor Q_1 turns on and supplies the extra current required. Since $V_{EB\ (ON)}$ remains fairly constant, the excess current comes from Q_1's base after amplification by β. The regulator adjusts I_B so that

$$I_L = I_c + I_o \tag{6.6}$$

and

$$I_c = \beta I_B \tag{6.7}$$

For the regulator,

$$I_o = I_i - I_Q$$
$$\simeq I_i \text{ (as } I_Q \text{ is small)} \tag{6.8}$$

Also

$$I_B = I_i - I_{R_1}$$
$$\simeq I_o - \frac{V_{EB\,(ON)}}{R_1} \tag{6.9}$$

Simplifying, we get

$$I_L = (\beta + 1) I_o - \beta \frac{V_{EB\,(ON)}}{R_1} \tag{6.10}$$

The maximum current $I_{o\,(max)}$ for a 7805 regulator is 1 A from the data sheet. Assuming $V_{EB\,(ON)}$ = 1 V and β = 15, we get from Eq. (6.10)

$$I_L = 16 \times 1 - 15 \times (1/7) = 13.8 \text{ A} \tag{6.11}$$

Example 6.1

In Fig. 6.4 (b), let $V_{EB\ (ON)}$ = 1 V and β = 15. Calculate the output current coming from 7805 and I_c coming from transistor Q_1 for loads 100 Ω, 5 Ω, 1 Ω.

Solution

Load = 100 Ω

For 7805, the output voltage across the load will be 5 V.

$$I_L = 5\text{V}/100\ \Omega = 0.05\text{ A} = 50\text{ mA}$$

The voltage across R_1 is 7 Ω × 50 mA = 350 mV which is less than 0.7 V. Hence Q_1 is ***off***.

So,

$$I_L = I_o = I_i = 50\text{ mA}$$

and

$$I_c = 0.$$

Load = 5 Ω

$$I_L = 5\text{ V}/5\ \Omega = 1\text{ A}$$

Assume that the entire current comes through regulator and that Q_1 is ***off***. Now the voltage drop across R_1 is equal to 7 Ω × 1 A = 7 V. Thus our assumption is wrong and Q_1 is ***on***. Putting the values in Eq. (6.10), it can be found that

$$I_o = 196 \text{ mA}$$

$$I_c = 904 \text{ mA}$$

Load = 1 Ω

$$I_L = 5 \text{ V}/1 \Omega = 5 \text{ A}$$

Here also Q_1 is ***on***. Solving Eq. (6.10) for I_o, we get

$$I_o = 446 \text{ mA}$$

So, $$I_c = 4.55 \text{ A}$$

Fixed Regulator used as Adjustable Regulator

In the laboratory, one may need variable regulated voltages or a voltage that is not available as standard fixed voltage regulator. This can be achieved by using a fixed three terminal regulator as shown in Fig. 6.5. Note that the ground (GND) terminal of the fixed three terminal regulator is floating. The output voltage

$$V_o = V_R + V_{pot} = V_R + (I_Q + I_{R1})\, R_2 = V_R + I_Q R_2 + \frac{V_R}{R_1} R_2$$

or, $$V_o = (1 + R_2/R_1)\, V_R + R_2 I_Q \qquad (6.12)$$

where V_R is the regulated voltage difference between the OUT and GND terminals. The effect of I_Q is minimized by choosing R_2 small enough to minimize the term $I_Q R_2$. The minimum output voltage is the value of the fixed voltage available from the regulator. The LM117, 217, 317 positive regulators and LM137, 237, 337 negative regulators have been specially designed to be used for obtaining adjustable output voltages. It is possible to adjust output voltage from 1.2 V to 40 V and current upto 1.5 A.

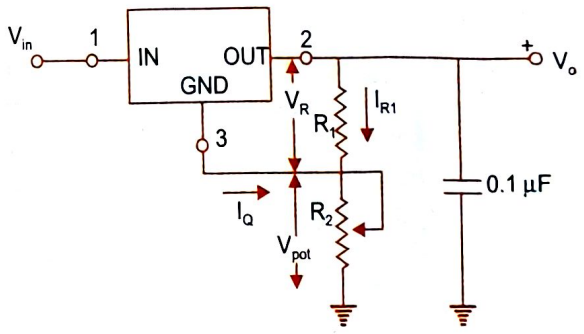


Fig. 6.5 Adjustable regulator

Example 6.2

Specify suitable component values to get $V_o = 7.5$ V in the circuit of Fig. 6.5 using a 7805 regulator.

Solution

From the data sheet of 7805, $I_Q = 4.2$ mA. Say, we choose $I_{R_1} = 25$ mA.

As $$V_R = 5 \text{ V for 7805},$$

$$R_1 = 5 \text{ V}/25 \text{ mA} = 200 \Omega$$

We have to choose R_2 so as to develop a voltage of 2.5 V across it. So,

$$R_2 = 2.5 \text{ V}/(I_{R_1} + I_Q) = 2.5/(4.2 + 25) = 85.6 \Omega$$

Choose $$R_2 = 85 \Omega$$

Dual Voltage Supply

Many discrete and IC circuits (such as op-amp) require bipolar (dual or ±V) supplies. This can be easily done with two three-terminal regulators. Figure 6.6 shows a bipolar ±15 V supply that can give 1 A from both (+) and (–) terminals. LM 340–15 is a +15V regulator with load current capability upto 1.5 A. The LM 320–15 is a –15 V regulator. It may be noted that the pin configuration of LM 340 and LM 320 is different. The diodes D_1 and D_2 in the circuit protect the regulator against short circuit occurring at its input terminals. Diodes D_3 and D_4 provide protection against the situation when both the regulators may not turn on simultaneously. If there is a load between the two outputs, the faster one will try to reverse the polarity of the other and cause it to latch up unless it is properly clamped. This clamping function is done by the diodes. Once the regulator start operating properly, both diodes will be reverse biased and will no longer have any effect on the circuit.

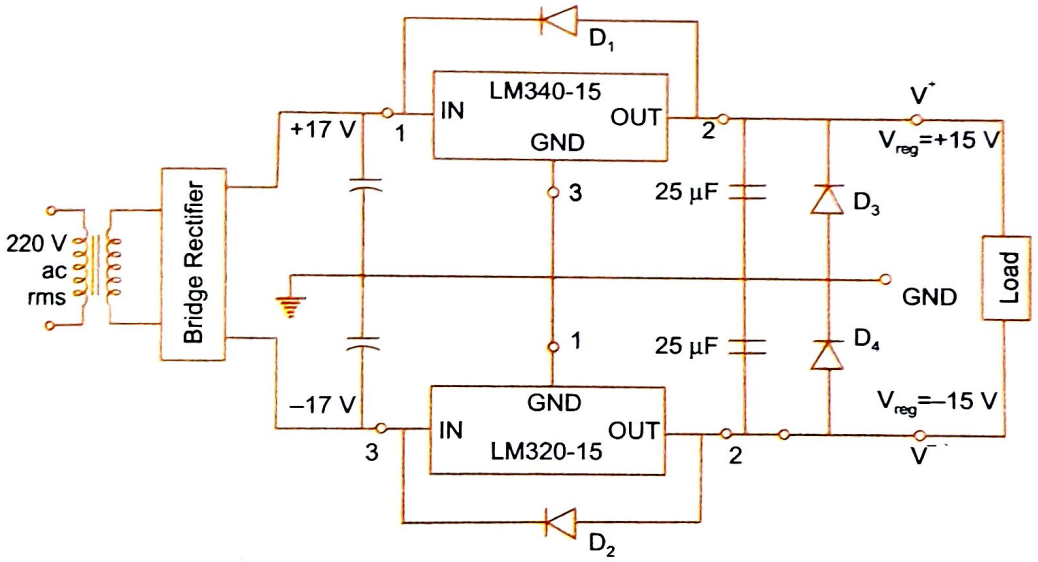


Fig. 6.6 A dual voltage (±15 V) supply

An op-amp draws less than 5 mA current, so a 100 mA supply can be used to drive a circuit consisting of 20 op-amps. LM 325H is a dual tracking ± 15V supply and is available in a 10-pin metal-can package and can furnish current upto 100 mA.

6.4 723 GENERAL PURPOSE REGULATOR

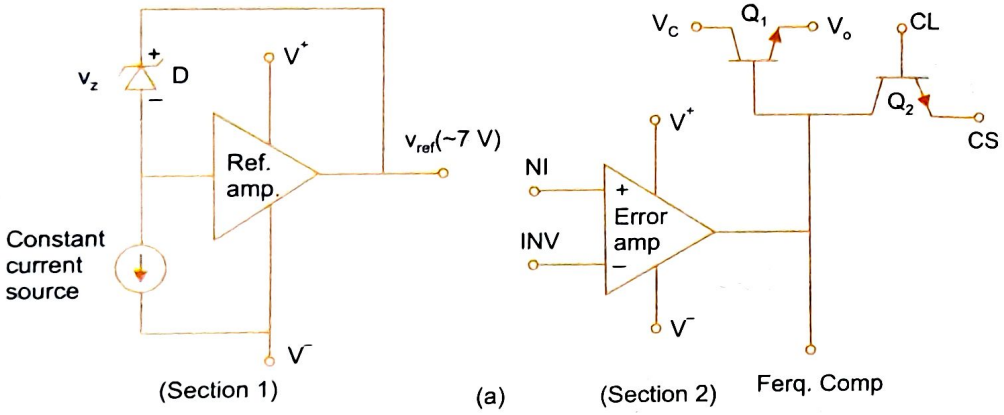
The three terminal regulators discussed earlier have the following limitations:

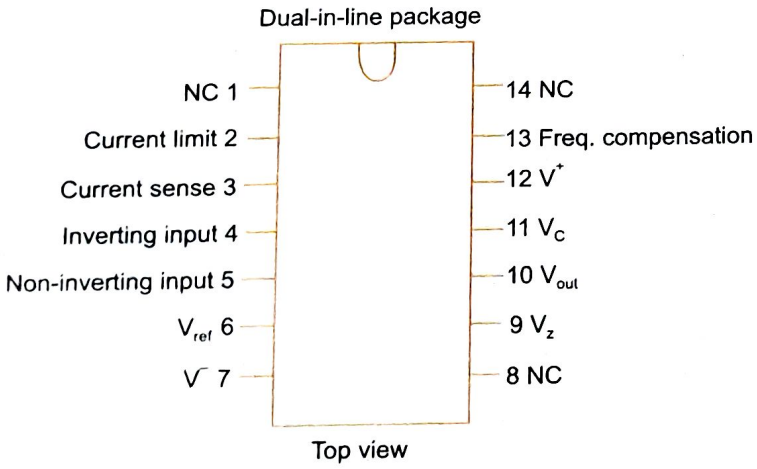
1. No short circuit protection
2. Output voltage (positive or negative) is fixed.

These limitations have been overcome in the 723 general purpose regulator, which can be adjusted over a wide range of both positive or negative regulated voltage. This IC is inherently low current device, but can be boosted to provide 5 amps or more current by connecting external components. The limitation of 723 is that it has no in-built thermal protection. It also has no short circuit current limits.

Figure 6.7 (a) shows the functional block diagram of a 723 regulator IC. It has two separate sections. The zener diode, a constant current source and reference amplifier produce a fixed voltage of about 7 volts at the terminal V_{ref}. The constant current source forces the zener to operate at a fixed point so that the zener outputs a fixed voltage.

The other section of the IC consists of an error amplifier, a series pass transistor Q_1 and a current limit transistor Q_2. The error amplifier compares a sample of the output voltage applied at the INV input terminal to the reference voltage V_{ref} applied at the NI input terminal. The error signal controls the conduction of Q_1. These two sections are not internally connected but the various points are brought out on the IC package. 723 regulated IC is available in a 14-pin dual-in-line package or 10-pin metal-can as shown in Fig. 6.7 (b). The important features and electrical characteristics are given in Table 6.2.





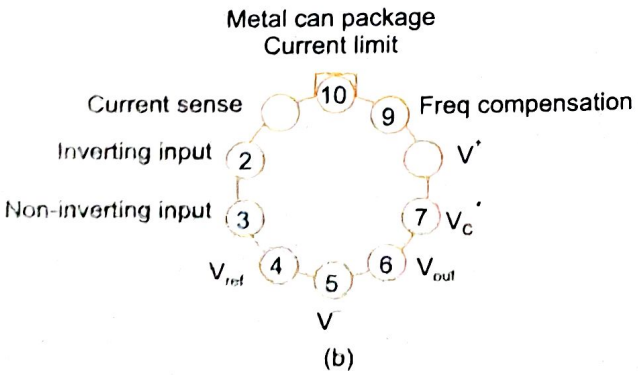


Fig. 6.7 (a) Functional block diagram of 723 regulator
(b) Pin diagram for 14-pin DIP and 10-pin metal-can

Table 6.2 723 IC regulator electrical characteristics

723 Voltage Regulator

Important Features:

*Input voltage 40 V max

*Output voltage adjustable from 2 V to 37 V

*150 mA output current without external pass transistor

*Output currents in excess of 10 A possible by adding external transistors

*Can be used as either a linear or a switching regulator

Parameter	*Conditions*	*LM723*			*LM723C*			*Units*
		Min	*Typ*	*Max*	*Min*	*Typ*	*Max*	
Line Regulation	V_{IN} = 12 V to V_{IN} = 15 V		.01	0.1		.01	0.1	% V_o
	$-55°C \le T_A \le +125°C$			0.3				% V_o
	$0°C \le T_A \le +70°C$						0.3	% V_o
	V_{IN} = 12 V to V_{IN} = 40 V		.02	0.2		0.1	0.5	% V_o
Load Regulation	I_L = 1 mA to I_L = 50 mA		.03	0.15		.03	0.2	% V_o
	$-55°C \le T_A \le +125°C$			0.6				% V_o
	$0°C \le T_A \le +70°C$						0.6	% V_o
Ripple Rejection	f = 50 Hz to 10 kHz, C_{REF} = 0		74			74		dB
	f = 50 Hz to 10 kHz, C_{REF} = 5 μF	86			86			dB
Average Temperature Coefficient of Output Voltage	$-55°C \le T_A \le +125°C$		.002	.015				%/°C
	$0°C \le T_A \le +70°C$					.003	.015	%/°C
Short Circuit Current Limit	R_{SC} = 10 Ω, V_{OUT} = 0		65			65		mA
Reference Voltage		6.95	7.15	7.35	6.80	7.15	7.50	V
Output Noise Voltage	BW = 100 Hz to 10 kHz, C_{REF} = 0		20			20		μV_{rms}
	BW = 100 Hz to 10 kHz, C_{REF} = 5 μF	2.5			2.5			μV_{rms}
Long Term Stability			0.1			0.1		%/1000 hrs
Standby Current Drain	I_L = 0, V_m = 30 V		1.3	3.5		1.3	4.0	mA
Input Voltage Range		9.5		40	9.5		40	V
Output Voltage Range		2.0		37	2.0		37	V
Input Output Voltage Differential		3.0		38	3.0		38	V

A simple positive low-voltage (2 V to 7 V) regulator can be made using 723 as shown in the schematic of Fig. 6.8 (a). In order to understand the circuit operation, consider the detailed circuit of Fig. 6.8 (b). The voltage at the NI terminal of the error amplifier due to R_1R_2 divider is,

$$V_{NI} = V_{ref} \frac{R_2}{R_1 + R_2} \tag{6.13}$$

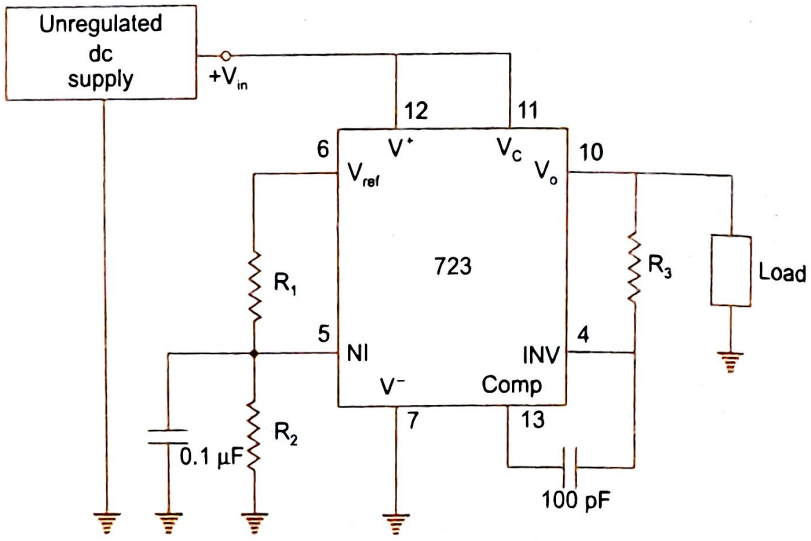


Fig. 6.8 (a) A low voltage regulator using 723 IC

The difference between V_{NI} and the output voltage V_o which is directly fed back to the INV terminal is amplified by the error amplifier. The output of the error amplifier drives the pass transistor Q_1 so as to minimize the difference between the NI and INV inputs of error amplifier. Since Q_1 is operating as an emitter follower

$$V_o = V_{ref} \frac{R_2}{R_1 + R_2} \tag{6.14}$$

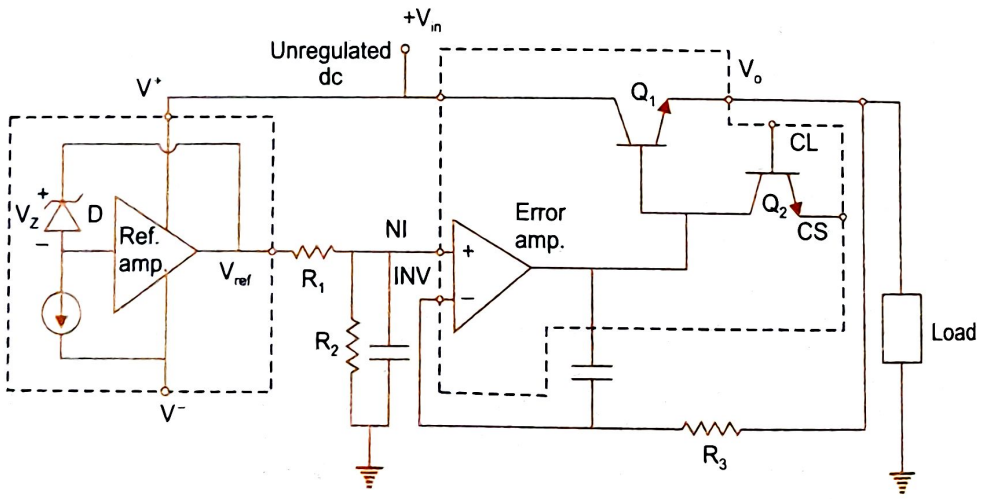


Fig. 6.8 (b) Functional diagram for a low voltage regulator

$V_{ref} \simeq 7$ V, $V_o = V_{NI} = 7R_2/(R_1 + R_2)$, $V^+ = +V_{cc}$, $R_3 = R_1 || R_2$ (minimum drift), $V^- =$ GND

If the output voltage becomes low, the voltage at the INV terminal of error amplifier also goes down. This makes the output of the error amp to become more positive, thereby driving transistor Q_1 more into conduction. This reduces the voltage across Q_1 and drives more current into the load causing voltage across load to increase. So the initial drop in the load voltage has been compensated. Similarly, any increase in load voltage, or changes in the input voltage get regulated.

The reference voltage is typically 7.15 V. So the output voltage V_o is

$$V_o = 7.15 \times \frac{R_2}{R_1 + R_2} \tag{6.15}$$

which will always be less than 7.15 V. So in the circuit of Fig. 6.8 (a) is used as low voltage (<7 V) 723 regulator.

If it is desired to produce regulated output voltage greater than 7 V, then the circuit of Fig. 6.8 (c) can be used. The NI terminal is connected directly to V_{ref} through R_3. So the voltage at the NI terminal is V_{ref}. The error amplifier operates as a non-inverting amplifier with a voltage gain of

$$A_v = 1 + \frac{R_1}{R_2} \tag{6.16}$$

So the output voltage for the circuit is

$$V_o = 7.15\left(1 + \frac{R_1}{R_2}\right) \tag{6.17}$$

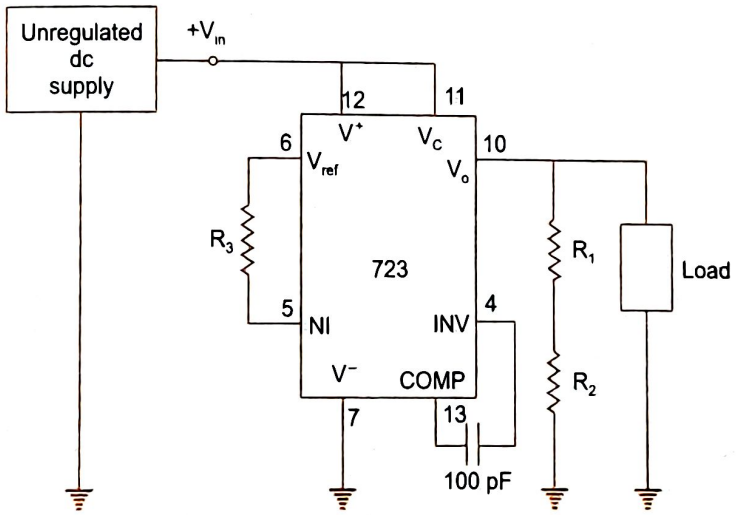


Fig. 6.8 (c) Basic high voltage 723 regulator

$V_{ref} = 7$ V, $V_o = 7(1 + R_1/R_2)$, $R_3 = R_1R_2$, $V^+ = +V_{cc}$, $V^- =$ GND

Current Limit Protection

The circuits of Fig. 6.8 have no protection. If the load demands more current *e.g.*, under short circuit conditions, the IC tries to provide it at a constant output voltage getting hotter all the time. This may ultimately burn the IC.

The IC is, therefore, provided with a current limit facility. Current limiting refers to the ability of a regulator to prevent the load current from increasing above a present value. The characteristic curve of a current limited power supply is shown in Fig. 6.9 (a). The output voltage remains constant for load current below I_{limit}. As current approaches to the limit, the output voltage drops. The current limit I_{limit} is set by connecting an external resistor R_{sc} between the terminals *CL* and *CS* terminals as shown in Fig. 6.9 (b). The *CL* terminal is also connected to the output terminal V_o and *CS* terminal to the load.

The load current produces a small voltage drop V_{sense} across R_{sc}. This voltage V_{sense} is applied directly across the base emitter junction of Q_2. When this voltage is approximately 0.5 volt, transistor Q_2 begins to turn ON. Now a part of the current from error amplifier goes to the collector of Q_2, thereby decreasing the base current of Q_1. This in turn, reduces the emitter current of Q_1. So any increase in the load current will get nullified. Similarly, if the load current decreases, V_{BE} of Q_2 drops, repeating the cycle in such a manner that the load current is held constant to produce a voltage across R_{sc} sufficient to turn ON Q_2. This voltage is typically 0.5 V.

$$\text{So,} \qquad I_{limit} = \frac{V_{sense}}{R_{sc}} \approx \frac{0.5\text{ V}}{R_{sc}} \tag{6.18}$$

This method of current limiting is also referred to as current sensing technique.

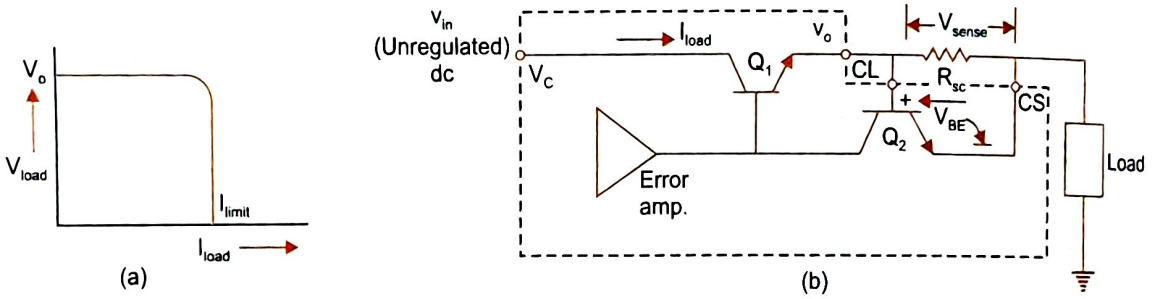


Fig. 6.9 (a) Characteristic curve for a current limited regulator (b) Current limit protection circuit

Current Foldback

In current limiting technique, the load current is maintained at a present value and when overload condition occurs, the output voltage V_o drops to zero. However, if the load is short circuited, maximum current does flow through the regulator. To protect the regulator, one must devise a method which will limit the short circuit current and yet allow higher currents to the load.

Current foldback is the method used for this. Figure 6.10 (a) shows the current foldback characteristic curve. As current demand increases, the output voltage is held constant till a present current level (I_{knee}) is reached. If the current demand exceeds this level, both output voltage and output current decrease. The circuit in Fig. 6.10 (b) shows the method of applying current foldback. In order to understand the operation of the circuit, consider the circuit of Fig. 6.10 (c). The voltage at terminal CL is divided by $R_3 - R_4$ network. The current limit transistor Q_2 conducts only when the drop across the resistance R_{sc} is large enough to produce a base-emitter voltage of Q_2 to be at least 0.5 V. As Q_2 starts conducting, transistor Q_1 begins to turn off and the current I_L decreases. This reduces the voltage V_1 at the emitter of Q_1 and also the output voltage V_o. The voltage at the base of Q_2 (CL) will be $V_1R_4/(R_3 + R_4)$. Thus the voltage at the CL terminal drops by a smaller amount compared to the drop in voltage at CS terminal. This increases V_{BE} of Q_2 thereby increasing the conduction of Q_2, which in turn reduces the conduction of Q_1. That is, the current I_L further reduces. This process continues till $V_o = 0$ V and V_1 is just large enough to keep 0.5 V between CL and CS terminal. This point is I_{sc} and has been reduced by lowering both I_L and V_o.

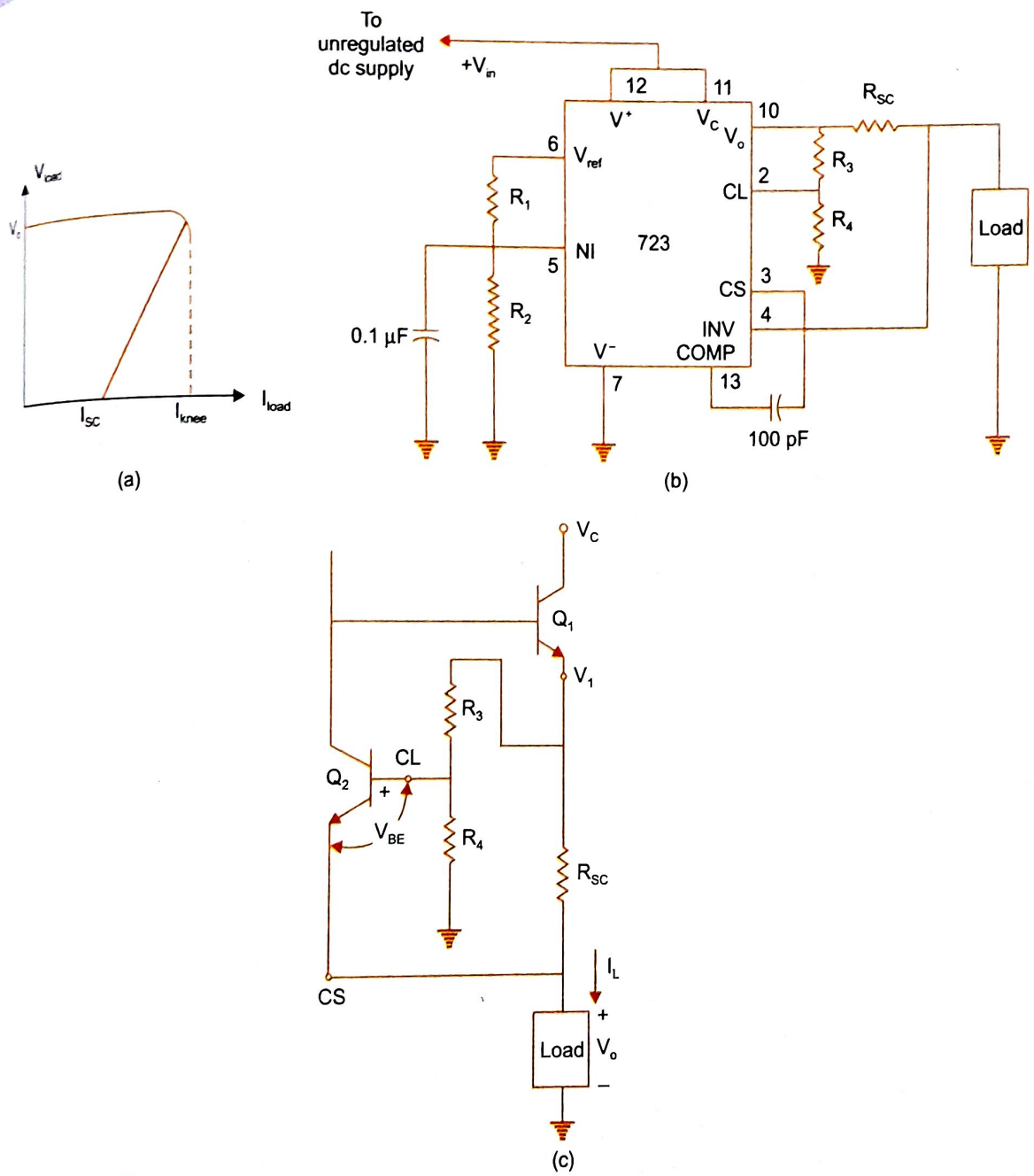


Fig. 6.10 (a) Current foldback characteristic curve (b) A low voltage regulator using current foldback (c) Current foldback (partial schematic)

Current Boosting

The maximum current that 723 IC regulator can provide is 140 mA. For many applications, this is not sufficient. It is possible to boost the current level simply by adding a boost transistor Q_1 to the voltage regulator as shown in Fig. 6.11. The collector current of the pass transistor Q_1 comes from the unregulated dc supply. The output current from V_o terminal drives the base of the pass transistor Q_1. This base current gets multiplied by the beta of the pass transistor, so that 723 has to provide only the base current. So,

$$I_{load} = \beta_{pass\ transistor} \times I_{o\ (723)} \tag{6.19}$$

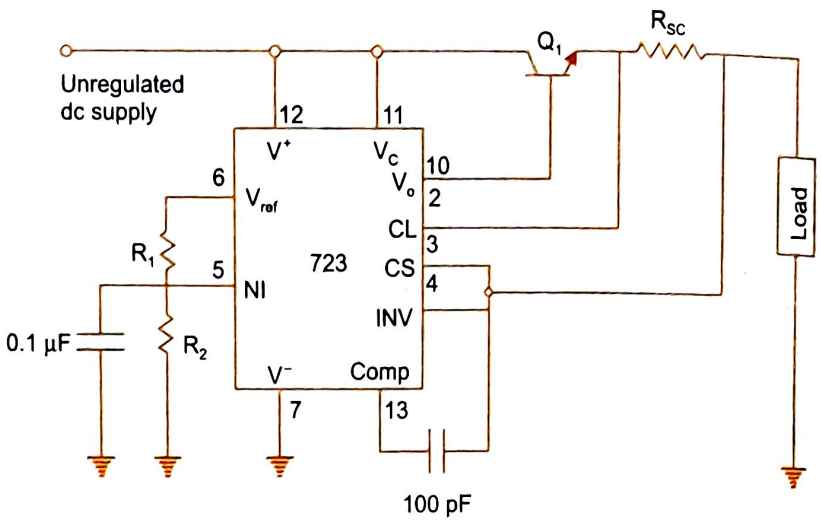


Fig. 6.11 Current boosted low voltage regulator

6.5 SWITCHING REGULATOR

The regulated power supplies discussed so far are referred to as linear voltage regulator, since the series pass transistor operates in the linear region. The linear voltage regulator has the following limitations.

The input stepdown transformer is bulky and the most expensive component of the linear regulated power supply mainly because of low line frequency (50 Hz). Because of the low line frequency, large values of filter capacitors are required to decrease the ripple. The efficiency of a series regulator is usually very low (typically 50 per cent). The input voltage must be greater than the output voltage. The greater the difference in input-output voltage, more will be the power dissipated in the series pass transistor which is always in the active region. A TTL system regulator (V_0 = 5 V) when operated at 10 V dc input gives 50 per cent efficiency and only 25 per cent for 20 V dc input. Another limitation is that in a system with one dc supply voltage (such as +5 V for TTL) if there is need for ±15 V for op-amp operation, it may not be economically and practically feasible to achieve this.

Switched mode power supplies overcome these difficulties. The switching regulator, also called switched mode regulator operate in a significantly different way from that of a conventional series regulator circuit discussed earlier. In series regulator, the pass transistor is operated in its linear region to provide a controlled voltage drop across it with a steady dc current flow. Whereas, in the case of switched-mode regulator, the pass transistor is used as a "controlled switch" and is operated at either cutoff or saturated state. Hence the power transmitted across the pass device is in discrete pulses rather than as a steady current flow. Greater efficiency is achieved since the pass device is operated as a low impedance switch. When the pass device is at cutoff, there is no current and dissipates no power. Again when the pass device is in saturation, a negligible voltage drop appears across it and thus dissipates only a small amount of average power, providing maximum current to the load. In either case, the power wasted in the pass device is very little and almost all the power is transmitted to the load. Thus efficiency in switched mode power supply is remarkably high–in the range of 70–90%.

Switched mode regulators rely on pulse width modulation to control the average value of the output voltage. The average value of a repetitive pulse waveform depends on the area

under the waveform. If the duty cycle is varied as shown in Fig. 6.12, the average value of the voltage changes proportionally.

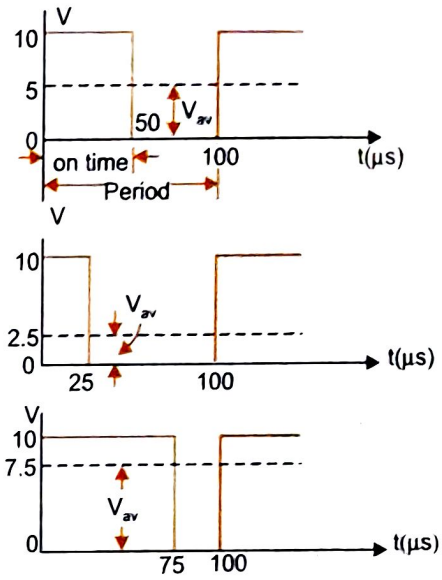


Fig. 6.12 Pulse width modulation and average value

A switching power supply is shown in Fig. 6.13. The bridge rectifier and capacitor filters are connected directly to the ac line to give unregulated dc input. The thermistor R_t limits the high initial capacitor charge current. The reference regulator is a series pass regulator of the type shown in Fig. 6.1. Its output is a regulated reference voltage V_{ref} which serves as a power supply voltage for all other circuits. The current drawn from V_{ref} is usually very small (~10 mA), so the power loss in the series pass regulator does not affect the overall efficiency of the switched mode power supply (SMPS). Transistors Q_1 and Q_2 are alternately switched ***off*** and ***on*** at 20 kHz. These transistors are either fully ***on*** ($V_{CE\ sat}$ ~ 0.2 V) or cut-off, so they dissipate very little power. These transistors drive the primary of the main transformer. The secondary is centre-tapped and full wave rectification is achieved by diodes D_1 and D_2. This unidirectional square wave is next filtered through a two stage LC filter to produce output voltage V_0.

The regulation of V_0 is achieved by the feedback circuit consisting of a pulse-width modulator and steering logic circuit. The output voltage V_0 is sampled by a R_1R_2 divider and a fraction

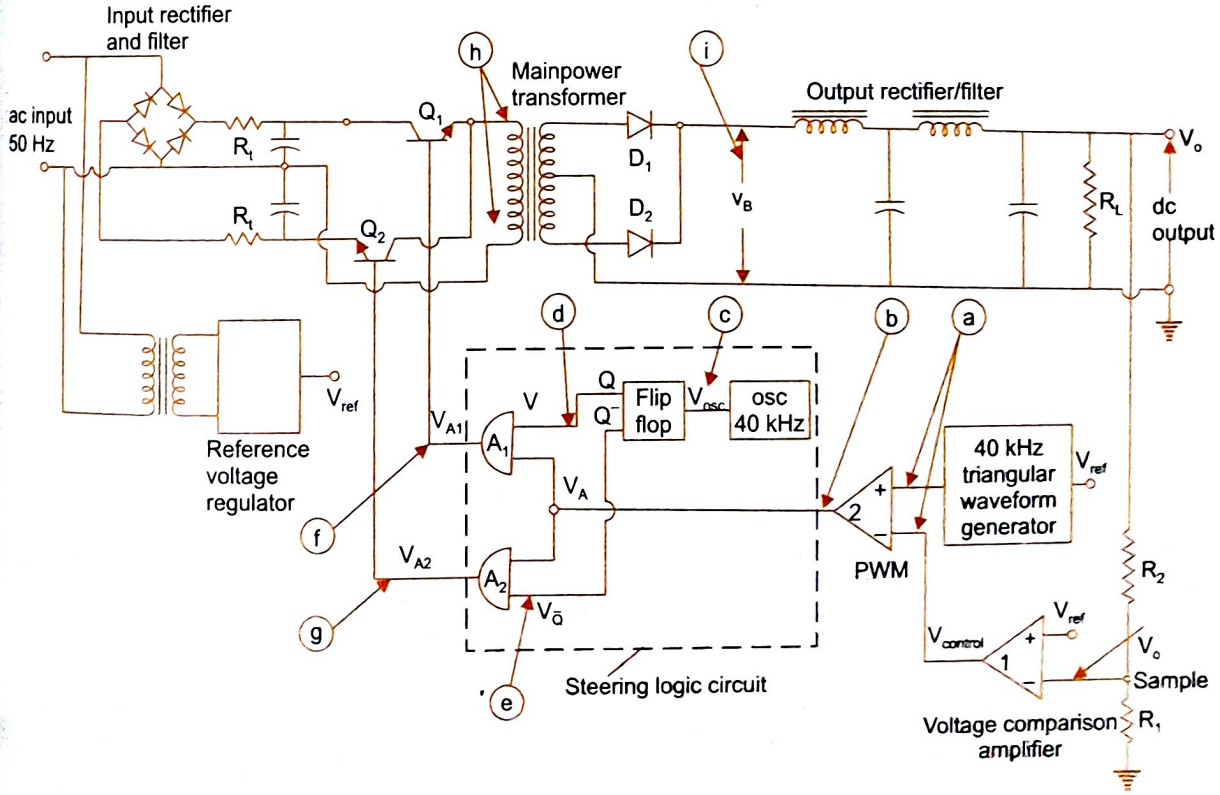


Fig. 6.13 A switched mode power supply

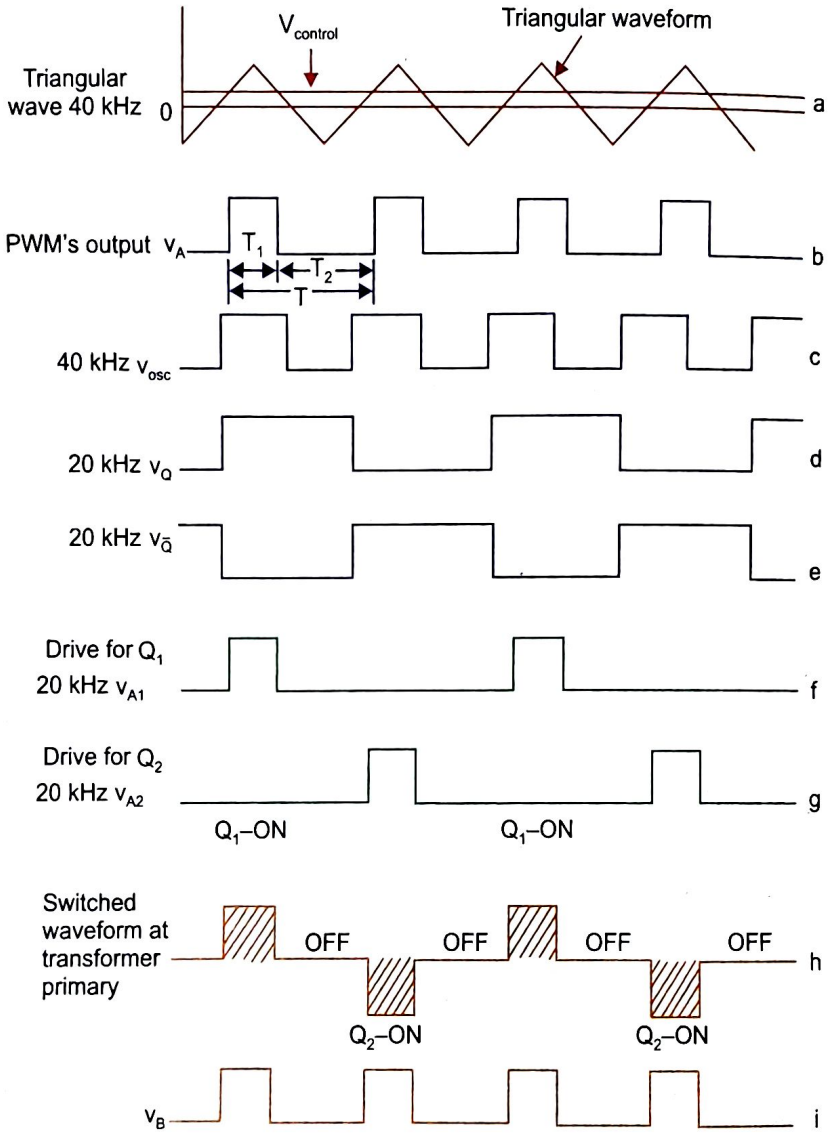


Fig. 6.14 Switching power supply waveforms

$R_1/(R_1+R_2)$ is compared with a fixed reference voltage V_{ref} in comparator 1. The output of this voltage comparison amplifier is called $V_{control}$ and is shown in Fig. 6.14 (a). $V_{control}$ is applied to the (–) input terminal of comparator 2 and a triangular waveform of frequency 40 kHz (also shown in Fig. 6.14 (a)) is applied at the (+) input terminal. It may be noted that a high frequency triangular waveform is being used to reduce the ripple. The comparator 2 functions as a pulse width modulator and its output is a square wave v_A (Fig. 6.14 (b)) of period T(f = 40 kHz). The duty cycle of the square wave is $T_1/(T_1 + T_2)$ and varies with $V_{control}$ which in turn varies with the variation of v_0. The output v_A drives a steering logic circuit shown in the dashed block. It consists of a 40 kHz oscillator cascaded with a flip-flop to produce two complementary outputs v_Q and $v_{\bar{Q}}$ shown in Fig. 6.14 (d) and (e). The output v_{A1} and v_{A2} of AND gates A_1 and A_2 are shown in Fig. 6.10 (f) and (g). These waveforms are applied at the base of transistor Q_1 and Q_2. Depending upon whether transistor Q_1 or Q_2 is ***on***, the waveform at the input of the transformer will be a square wave as shown in Fig. 6.14 (h). The rectified output v_B is shown in Fig. 6.14 (i).

An inspection of Fig. 6.13 shows that the output current passes through the power switch consisting of transistors Q_1 and Q_2, inductor having low resistance and the load. Hence using a switch with low losses (transistor with small $V_{CE\,(sat)}$ and high switching speed) and a filter with high quality factor, the conversion efficiency can easily exceed 90%.

If there is a rise in dc output voltage V_o, the voltage control $V_{control}$ of the comparator 1 also rises. This changes the intersection of the $V_{control}$ with the triangular waveform and in this case decreases the time period T_1 in the waveform of Fig. 6.14 (b). This in turn decreases the pulse width of the waveform driving the main power transformer. Reduction in pulse width lowers the average value of the dc output V_o. Thus the initial rise in the dc output voltage V_o has been nullified.

So far we have discussed the operation of the SMPS. Now we shall be able to justify why SMPS has better efficiency than linear regulated power supply. We have noted that very high frequency signals (about 40 kHz or more) are being applied. The transistors Q_1 and Q_2 are acting as the switches and become alternately ***on*** and ***off*** at a frequency of 20 kHz (Fig. 6.14 (a)). Again the transistor Q_1 or Q_2 is ***on*** for very small duration and consumes negligibly small power since $V_{CE\,(sat)}$ (0.2 V) is small. It may also be noted that the high operating frequency used for the switching transistors allows the use of smaller transformers, capacitors and inductors. This allows a decrease in size and cost.

There are some limitations and precautions to be taken with switching power supplies. Since the rectifier is tied directly to the ac line voltage, the rectifiers, capacitors and switching transistors must be able to withstand the peak line voltage (310 V for 220 V ac rms line). The resistor R_t must be provided to prevent the uncharged capacitors from shorting out the line when initially turned on. A switched mode power supply is more complex and requires external components like inductors and transformers. It is slow in responding to transient load changes compared to the conventional series regulator. One should be careful about the electromagnetic and radio-frequency interference while using switched mode power supply.

As can be seen, the switching regulator system is quite a complex one. However, with modern microelectronics, quite a few packages are available. The Motorola MC 3420/3520 is a pulse width modulator IC chip. The Silicon General SG 1524 produces an IC package containing reference regulator, pulse width modulator (consisting of saw tooth oscillator and comparator), comparator 1, transistors Q_1 and Q_2, the steering flip-flop and two AND gates.

SUMMARY

1. A regulated power supply provides a dc voltage independent of the load current, temperature and ac line voltage variations.
2. A regulated power supply has four parts: reference voltage circuit, error amplifier, a series-pass transistor and a feed back network.
3. There are several IC regulators available. 78 XX/79 XX series are three terminal positive and negative fixed voltage regulators.
4. The IC regulators combine the reference voltage source, error op-amp, pass transistor with short circuit current limiting and thermal overload protection.
5. The 723 regulator can give adjustable output voltage in a wide range. It provides short circuit protection and current foldback using external components. The basic regulator can be current boosted with an external pass transistor.
6. The switching power supply allows a decrease in size and cost. The pass transistors

here are switched ON and OFF at 20 kHz or faster. The output level is controlled by varying the pulse width of the switching waveform. Operating at this frequency allows the use of smaller transformers, capacitors and inductors.

REVIEW QUESTIONS

6.1. What is the function of a voltage regulator?
6.2. Give the important parts of a series regulated power supply using discrete components.
6.3. What is a voltage reference? Why is it needed?
6.4. What is the function of a series pass transistor?
6.5. What voltage options are available in 78 XX and 79 XX voltage regulators?
6.6. Show the standard representation of IC voltage regulator.
6.7. List and explain the characteristics of three terminal IC regulators.
6.8. Explain the important parameters listed in the data sheet of 78 XX.
6.9. Explain the protections used in 78 XX.
6.10. What are the limitations of three terminal regulator?
6.11. Draw the functional diagram of 723 regulator.
6.12. Explain the current limiting feature of 723 regulator.
6.13. Explain current foldback characteristics.
6.14. How is current boosting achieved in a 723 IC?
6.15. Discuss the limitations of linear voltage regulators.
6.16. What is the principle of switch-mode power supplies? Discuss its advantages and disadvantages.

PROBLEMS

6.1. Using 7805 design a current source to deliver 0.2 A current to a 22 Ω, 10 W load.
6.2. Design a voltage regulator using 723 to get a voltage output of 3 V.
(Hint: See Fig. 6.8 (a), calculate R_1 and R_2)
6.3. Calculate the values of R_1 and R_2 for a high voltage 723 regulator of Fig. 6.8 (c) so as to get an output voltage of 28 volts.
6.4. Design a current limit circuit for a 723 regulator to limit the current to 60 mA.
6.5. Design an adjustable voltage regulator (3 volts to 28 volts) with a short circuit limit of 60 mA using a 723 regulator.
6.6. Design an adjustable regulator from the 7810 regulator to get an output voltage of 15 V.

EXPERIMENT

(a) To study a fixed three terminal voltage regulator.
(b) To study the operation of 723 regulator *IC*.
(c) To study current foldback circuit.

PROCEDURE (A)

(i) Connect a 7805 voltage regulator as shown in Fig. E. 6.1 (a).
(ii) Set the power supply voltage V_{in} to + 10 V dc. Measure and record the load current I_L and load voltage V_L for R_L: 220 Ω (1/4 W); 100 Ω (1/2 W); 22Ω (1 W); 22 Ω || 22 Ω = 11 Ω

(each resistor 2 W). Calculate per cent load regulation as the change in the load voltage V_L over some limited range of load current. Compare with the manufacturer's data.

(iii) To measure line regulation, connect the two 22 Ω parallel resistors as load and measure the load voltage V_L for V_{in} : +7 V dc, +12 V dc, +18 V dc. Calculate line regulation as the per cent change in output voltage for a change in the input voltage.

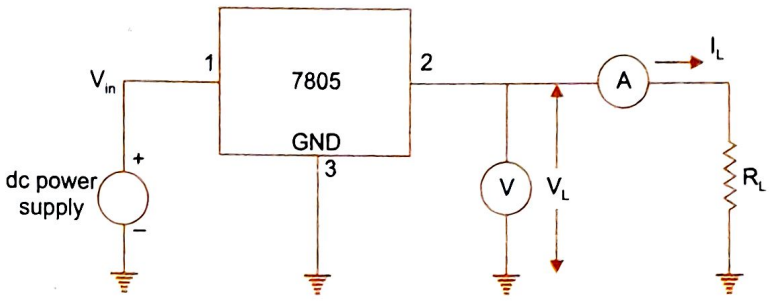


Fig. E. 6.1 (a) 7805 voltage regulator

(iv) With V_{in} set to +10 V dc, short the output terminal of the regulator to ground with a piece of heavy wire just for moment. Observe the short circuit current. After removing the short circuit verify that the regulator still operates properly and gives a stable output voltage.

PROCEDURE (B)

(i) Connect the 723 regulator as shown in Fig. E. 6.1 (b).

(ii) Set the dc power supply voltage V_{in} to +10 V. Measure and record V_{ref} with respect to ground. With load R_L (10 kΩ-pot) removed from the circuit (output open) measure the minimum and maximum output voltages by rotating the 1 kΩ-pot through its full range.

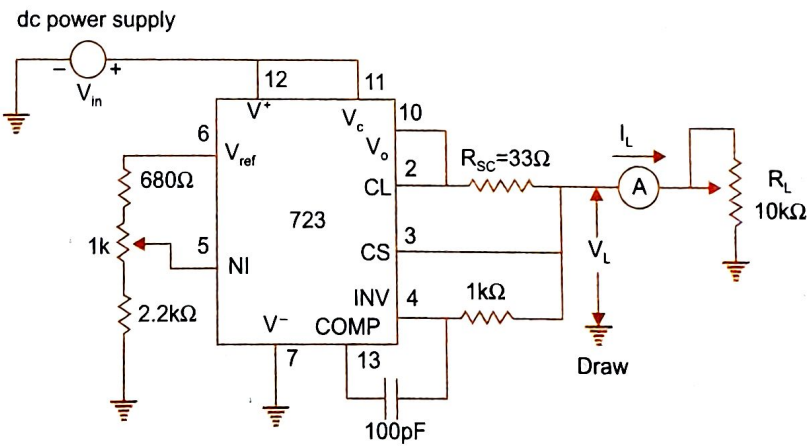


Fig. E. 6.1 (b) 723 voltage regulator

(iii) Now adjust the 1 kΩ-pot so that V_0 is +5 V dc. Measure the voltage between the wiper arm of the 1 kΩ-pot and ground.

(iv) Adjust the load R_L (10 kΩ-pot) until the load current I_L = 1 mA. Record V_L. Repeat for different values of load currents; 5 mA, 10 mA, 15 mA and 18 mA. Calculate load regulation and compare with the manufacturer's specifications.

(v) Gradually increase the load current above 18 mA. You will see that the load voltage suddenly decreases when the load current is about 18 to 20 mA. Now the voltage across R_{sc} is enough to begin current limiting. Measure and record a few values of load current and load voltage below and above the current limiting point. Plot a graph of V_L versus I_L from the data obtained in steps (iv) and (v).

11

D-A AND A-D CONVERTERS

11.1 INTRODUCTION

Most of the real-world physical quantities such as voltage, current, temperature, pressure and time etc. are available in analog form. Even though an analog signal represents a real physical parameter with accuracy, it is difficult to process, store or transmit the analog signal without introducing considerable error because of the superim-position of noise as in the case of amplitude modulation. Therefore, for processing, transmission and storage purposes, it is often convenient to express these variables in digital form. It gives better accuracy and reduces noise. The operation of any digital communication system is based upon analog to digital (A/D) and digital to analog (D/A) conversion.

Figure 11.1 highlights a typical application within which A/D and D/A conversion is used. The analog signal obtained from the transducer is band limited by antialiasing filter. The signal is then sampled at a frequency rate more than twice the maximum frequency of the band limited signal. The sampled signal has to be held constant while conversion is taking place in A/D converter. This requires that ADC should be preceded by a sample and hold (S/H) circuit. The ADC output is a sequence in binary digit. The micro-computer or digital signal processor performs the numerical calculations of the desired control algorithm. The D/A converter is to convert digital signal into analog and hence the function of DAC is exactly opposite to that of ADC. The D/A converter is usually operated at the same frequency as the ADC. The output of a D/A converter is commonly a staircase. This staircase-like digital output is passed through a smoothing filter to reduce the effect of quantization noise.

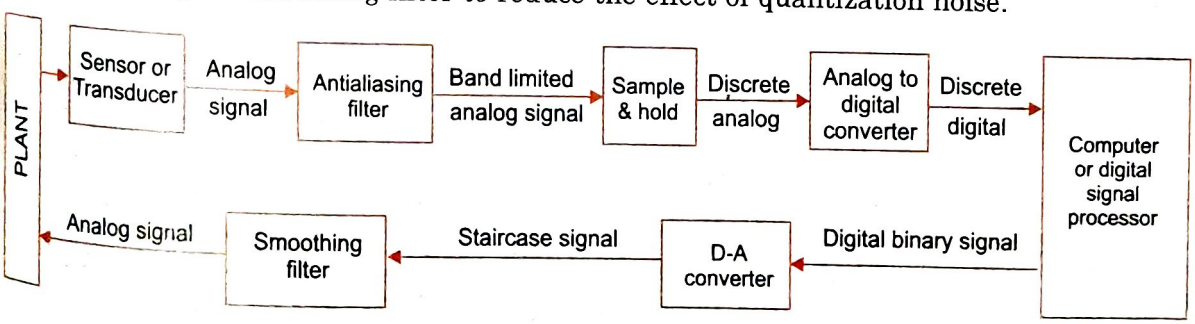


Fig. 11.1 Circuit showing application of A/D and D/A converter

The scheme given in Fig. 11.1 is used either in full or in part in applications such as digital audio recording and playback, computer, music and video synthesis, pulse code modulation transmission, data acquisition, digital multimeter, direct digital control, digital signal processing, microprocessor based instrumentation.

Both ADC and DAC are also known as data converters and are available in IC form. It may be mentioned here that for slowly varying signal, sometimes sample and hold circuit may be avoided without considerable error. The A-D conversion usually makes use of a D-A converter so we shall first discuss DAC followed by ADC.

11.2 BASIC DAC TECHNIQUES

The schematic of a DAC is shown in Fig. 11.2. The input is an n-bit binary word D and is combined with a reference voltage V_R to give an analog output signal. The output of a DAC can be either a voltage or current. For a voltage output DAC, the D/A converter is mathematically described as

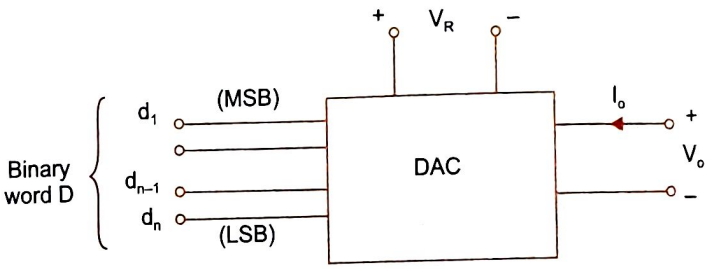


Fig. 11.2 Schematic of a DAC

$$V_o = K\, V_{FS}\,(d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n}) \tag{11.1}$$

where, V_o = output voltage

V_{FS} = full scale output voltage

K = scaling factor usually adjusted to unity

$d_1 d_2 \ldots d_n$ = n-bit binary fractional word with the decimal point located at the left

d_1 = most significant bit (MSB) with a weight of $V_{FS}/2$

d_n = least significant bit (LSB) with a weight of $V_{FS}/2^n$

There are various ways to implement Eq. (11.1). Here we shall discuss the following resistive techniques only:

Weighted resistor DAC

R-2R ladder

Inverted R-2R ladder

11.2.1 Weighted Resistor DAC

One of the simplest circuits shown in Fig. 11.3 (a) uses a summing amplifier with a binary weighted resistor network. It has n-electronic switches $d_1, d_2, \ldots, d_n$ controlled by binary input word. These switches are single pole double throw (SPDT) type. If the binary input to a particular switch is 1, it connects the resistance to the reference voltage ($-V_R$). And if the input bit is 0, the switch connects the resistor to the ground. From Fig. 11.3 (a), the output current I_o for an ideal op-amp can be written as

$$I_o = I_1 + I_2 + \ldots + I_n$$

$$= \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \ldots + \frac{V_R}{2^n R} d_n$$

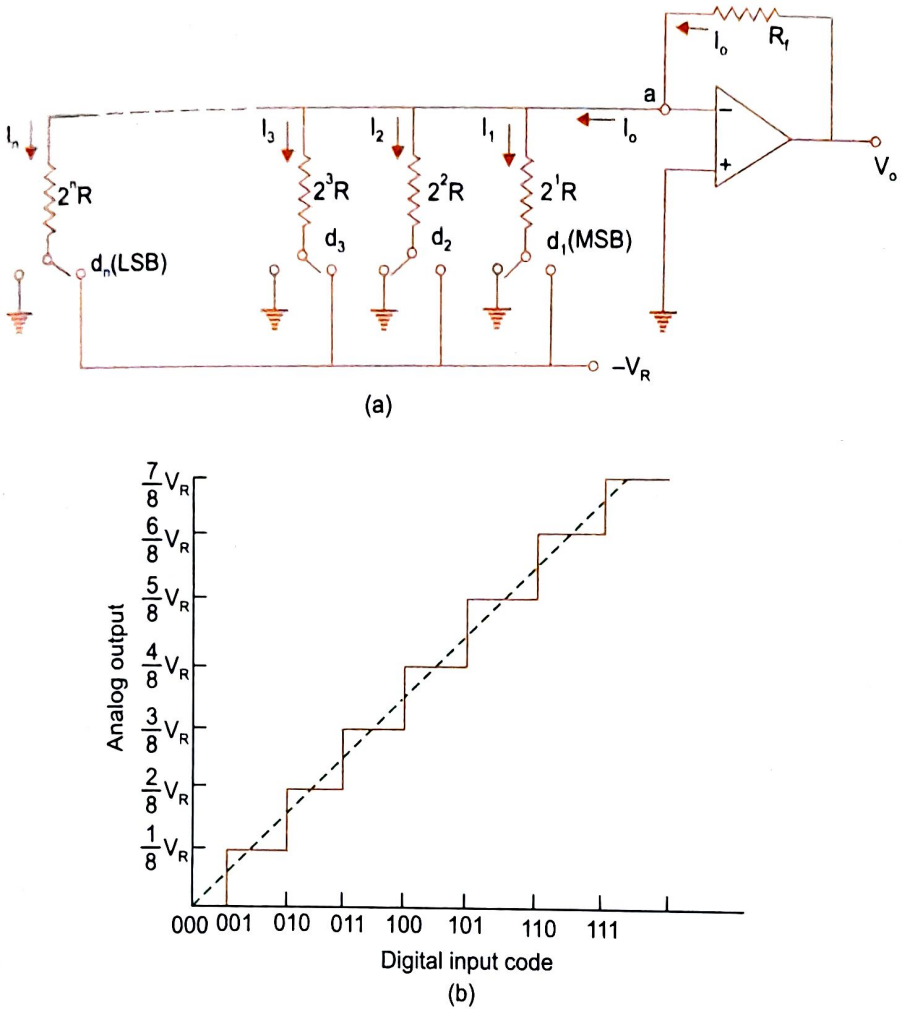


Fig. 11.3 (a) A simple weighted resistor DAC, (b) Transfer characteristics of a 3-bit DAC

$$= \frac{V_R}{R}(d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n})$$

The output voltage

$$V_o = I_o R_f = V_R \frac{R_f}{R}(d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n}) \quad (11.2)$$

Comparing Eq. (11.1) with Eq. (11.2), it can be seen that if $R_f = R$ then $K = 1$ and $V_{FS} = V_R$.

The circuit shown in Fig. 11.3 (a) uses a negative reference voltage. The analog output voltage is therefore positive staircase as shown in Fig. 11.3 (b) for a 3-bit weighted resistor DAC. It may be noted that

(i) Although the op-amp in Fig. 11.3 (a) is connected in inverting mode, it can also be connected in non-inverting mode.
(ii) The op-amp is simply working as a current to voltage converter.
(iii) The polarity of the reference voltage is chosen in accordance with the type of the switch used. For example, for TTL compatible switches, the reference voltage should be +5 V and the output will be negative.

The accuracy and stability of a DAC depends upon the accuracy of the resistors and the tracking of each other with temperature. There are however a number of problems associated with this type of DAC. One of the disadvantages of binary weighted type DAC is the wide range of resistor values required. It may be observed that for better resolution, the input binary word length has to be increased. Thus, as the number of bit increases, the range of resistance value increases. For 8-bit DAC, the resistors required are 2^0R, 2^1R, 2^2R, ..., 2^7R. The largest resistor is 128 times the smallest one for only 8-bit DAC. For a 12-bit DAC, the largest resistance required is 5.12 MΩ if the smallest is 2.5 kΩ. The fabrication of such a large resistance in IC is not practical. Also the voltage drop across such a large resistor due to the bias current would also affect the accuracy. The choice of smallest resistor value as 2.5 kΩ is reasonable; otherwise loading effect will be there. The difficulty of achieving and maintaining accurate ratios over such a wide range especially in monolithic form restricts the use of weighted resistor DACs to below 8-bits.

The switches in Fig. 11.3 (a) are in series with resistors and therefore, their ***on*** resistance must be very low and they should have zero offset voltage. Bipolar transistors do not perform well as voltage switches, due to the inherent offset voltage when in saturation. However, by using MOSFET, this can be achieved.

Different types of ***digitally controlled SPDT electronic switches*** are available of which two are shown in Fig. 11.4. A totem-pole MOSFET driver in Fig. 11.4 (a) feeds each resistor connected to the inverting input terminal 'a' of Fig. 11.3 (a). The two complementary gate inputs Q and $\overline{Q}$ come from MOSFET S-R flip-flop or a binary cell of a register which holds one bit of the digital information to be converted to an analog number. Assume a negative logic, i.e. logic '1' corresponds to – 10 V and logic '0' corresponds to zero volt. If there is '1' in the bit line, $S = 1$ and $R = 0$ so that $Q = 1$ and $\overline{Q} = 0$. This drives the transistor Q_1 ***on***, thus connecting the resistor R_1 to the reference voltage $-V_R$ whereas the transistor Q_2 remains ***off***. Similarly a '0' at the bit line connects the resistor R_1 to the ground terminal.

Another SPDT switch of Fig. 11.4(b) consists of CMOS inverter feeding an op-amp voltage follower which drives R_1 from a very low output resistance. The circuit is using a positive logic with $V(1) = V_R = +5$ V and $V(0) = 0$ V. The complement $\overline{Q}$ of the bit under consideration is applied at the input. Thus $\overline{Q} = 0$ makes transistor Q_1 ***off*** and Q_2 ***on***. The output of the CMOS inverter is at logic 1, that is, 5 V is applied to resistor R_1 through the voltage follower. And if $\overline{Q} = 1$ the output of the CMOS inverter is 0 V connecting the resistance R_1 to ground.

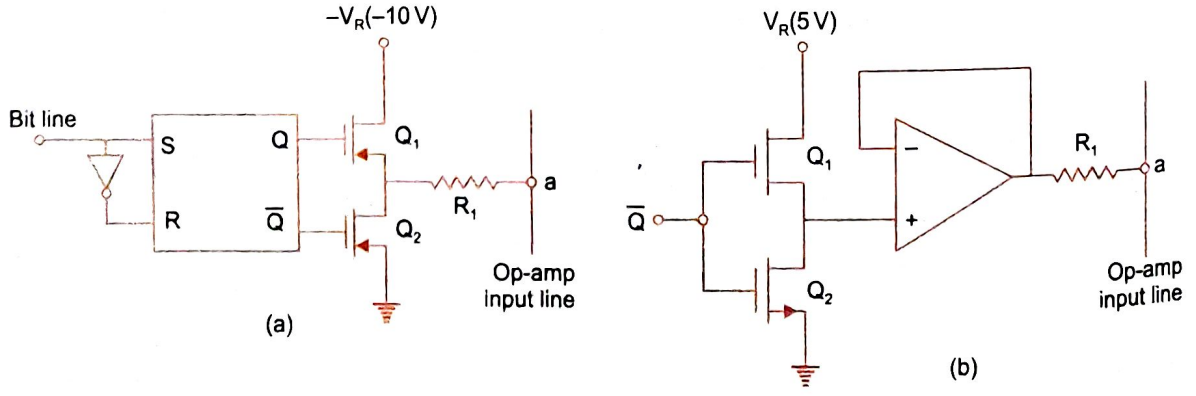


Fig. 11.4 (a) A totem pole MOSFET switch (b) CMOS inverter as switch

11.2.2 R-2R Ladder DAC

Wide range of resistors are required in binary weighted resistor type DAC. This can be avoided by using R-2R ladder type DAC where only two values of resistors are required. It is well suited for integrated circuit realization. The typical value of R ranges from 2.5 kΩ to 10 kΩ.

For simplicity, consider a 3-bit DAC as shown in Fig. 11.5 (a), where the switch position $d_1\, d_2\, d_3$ corresponds to the binary word 100. The circuit can be simplified to the equivalent form of Fig. 11.5 (b) and finally to Fig. 11.5 (c). Then, voltage at node C can be easily calculated by the set procedure of network analysis as

$$\frac{-V_R\left(\frac{2}{3}R\right)}{2R+\frac{2}{3}R} = -\frac{V_R}{4}$$

The output voltage is

$$V_0 = \frac{-2R}{R}\left(-\frac{V_R}{4}\right) = \frac{V_R}{2} = \frac{V_{FS}}{2}$$

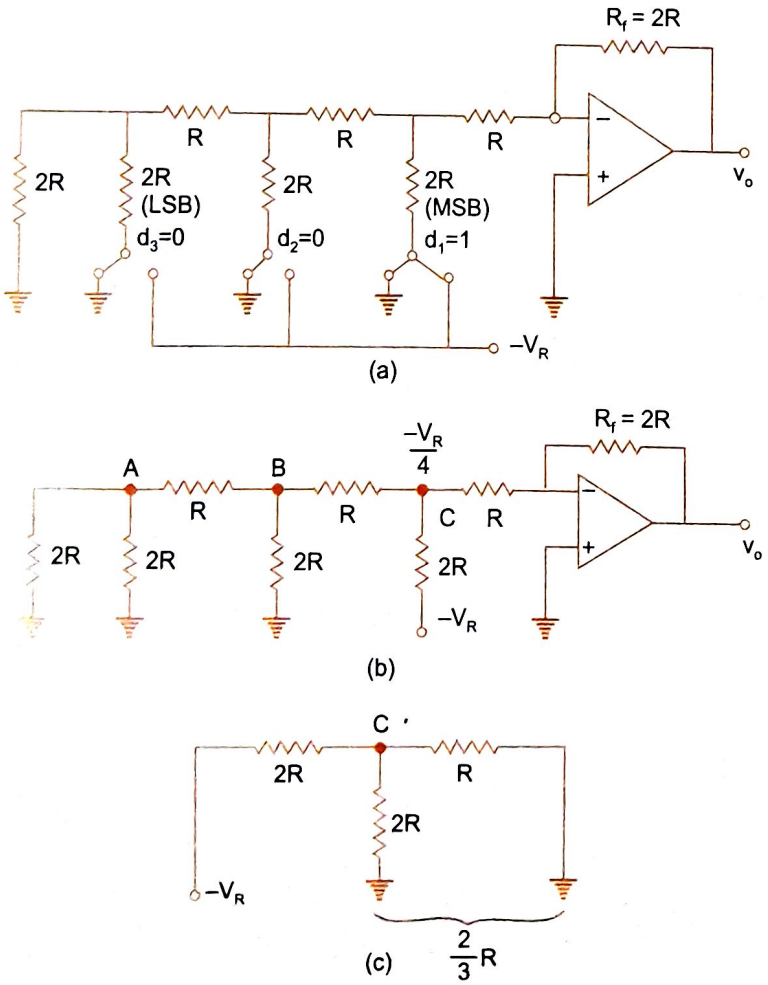


Fig. 11.5 (a) R-2R ladder DAC, (b) Equivalent circuit of (a), (c) Equivalent circuit of (b)

The switch position corresponding to the binary word 001 in 3 bit DAC is shown in Fig. 11.6 (a). The circuit can be simplified to the equivalent form of Fig. 11.6 (b). The voltages at the nodes (A, B, C) formed by resistor branches are easily calculated in a similar fashion and the output voltage becomes

$$V_o = \left(-\frac{2R}{R}\right)\left(-\frac{V_R}{16}\right) = \frac{V_R}{8} = \frac{V_{FS}}{8}$$

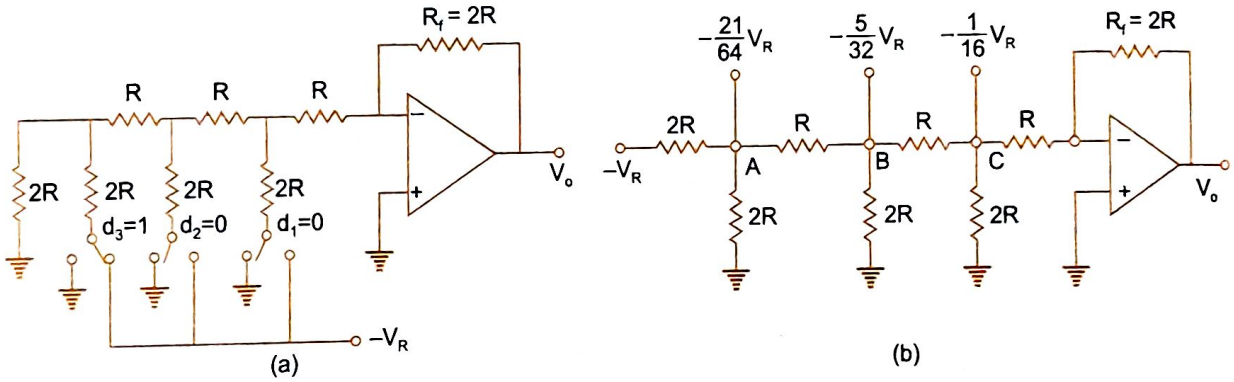


Fig. 11.6 (a) R-2R ladder DAC for switch positions 001, (b) Equivalent circuit

In a similar fashion, the output voltage for R-2R ladder type DAC corresponding to other 3-bit binary words can be calculated.

Example 11.1

Consider a 4 bit R-$2R$ ladder DAC of the type shown in Fig 11.5 (a). Given R = 10 KΩ and V_R = 10 V. Determine the value of the feedback resistance R_f for the following output conditions.

(i) value of 1 LSB at the output is 0.5V
(ii) analog output is 6V for a binary input of 1000
(iii) full scale output voltage is 10 V

Solution

(i) Given R = 10 KΩ, V_R = 10V and n = 4
The resolution of a $R - 2R$ ladder DAC is given by

$$\text{Resolution, } V = \frac{1}{2^n} \times \frac{V_R}{R} \times R_f$$

Thus
$$0.5V = \frac{1 \times 10V \times R_f}{2^4 \times 10 \times 10^3}$$

or
$$R_f = 8 \text{ K}\Omega$$

(ii) For binary digital input 1000, setting $d_1 = 1$ and $d_2 = d_3 = d_4 = 0$ in Fig 11.3(a), we can write

$$V_o = V_R \frac{R_f}{R}\left(d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + d_4 2^{-4}\right)$$

$$6 = \frac{R_f \times 10V \times 2^{-1}}{10 \times 10^3} \left(\text{as } d_2 = d_3 = d_4 = 0\right)$$

Therefore, $R_f = 12\ \text{K}\Omega$

(iii) Now $d_1 = d_2 = d_3 = d_4 = 1$. Thus for getting the full scale voltage of 10V,

$$R_f \times \frac{10}{10 \times 10^3}\left(2^{-1} + 2^{-2} + 2^{-3} + 2^{-4}\right) = 10$$

Thus $R_f = 10.667\ \text{K}\Omega$

11.2.3 Inverted R-2R Ladder

In weighted resistor type DAC and R-2R ladder type DAC, current flowing in the resistors changes as the input data changes. More power dissipation causes heating, which in turn, creates non-linearity in DAC. This is a serious problem and can be avoided completely in 'Inverted R-2R ladder type DAC'. A 3-bit Inverted R-2R ladder type DAC is shown in Fig. 11.7 (a) where the position of MSB and LSB is interchanged. Here each input binary word connects the corresponding switch either to ground or to the inverting input terminal of the op-amp which is also at virtual ground. Since both the terminals of switches d_i are at ground potential, current flowing in the resistances is constant and independent of switch position, i.e. independent of input binary word. In Fig. 11.7 (a), when switch d_i is at logical '0' i.e., to the left, the current through 2R resistor flows to the ground and when the switch d_i is at logical '1' i.e., to the right, the current through 2R sinks to the virtual ground. The circuit has the important property that the current divides equally at each of the nodes. This is because the equivalent resistance to the right or to the left of any node is exactly 2 R. The division of the current is shown in Fig. 11.7 (b). Consider a reference current of 2 mA. Just to the right of node *A*, the equivalent resistor is 2 R. Thus 2 mA of reference input current divides equally to value 1 mA at node *A*. Similarly to the right of node *B*, the equivalent resistor is 2 R. Thus 1 mA of current further divides to value 0.5 mA at node *B*. Similarly, current divides equally at node *C* to 0.25 mA. The equal division of current in successive nodes remains the same in the 'inverted R-2R ladder' irrespective of the input binary word. Thus the currents remain constant in each branch of the ladder. Since constant current implies constant voltage, the ladder node voltages remain constant at $V_R/2^0$, $V_R/2^1$, $V_R/2^2$. The circuit works on the principle of summing currents and is also said to operate in the current mode. The most important advantage of the current mode or inverted ladder is that since the ladder node voltages remain constant even with changing input binary words (codes), the stray capacitances are not able to produce slow-down effects on the performance of the circuit.

It may be noted that the switches used in Fig. 11.7 (a) are the SPDT switches discussed earlier. According to bit d_i, the corresponding switch gets connected either to ground for $d_i = 0$ or to $-V_R$ for $d_i = 1$. The current flows from inverting input terminal to $-V_R$ for $d_i = 1$ and from ground to $-V_R$ for $d_i = 0$. Regardless of the binary input word, the current in the resistive branches of the inverted ladder circuit remains always constant as explained in Fig. 11.7(b). However, the current through the feedback resistor R is the summing current depending upon the input binary word. It may further be mentioned that, Fig. 11.7 (b) shows only the current division for making the analysis simple, though it is a voltage driven DAC.

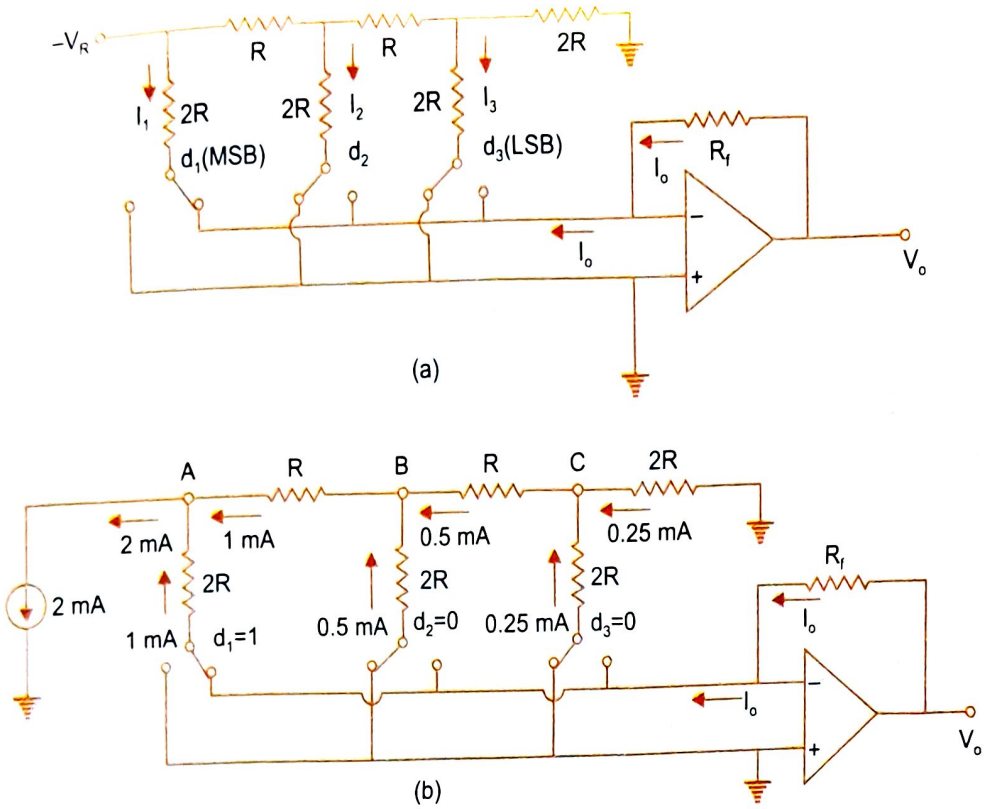


Fig. 11.7 (a) Inverted R-2R ladder DAC, (b) Inverted R-2R ladder DAC showing division of current for digital input word 001

Example 11.2

Consider the inverted $R - 2R$ ladder DAC shown in Fig 11.7 (a) Given $R = R_f = 10$ KΩ and $V_R = 10$V. Calculate the output voltage for the binary input of 1110.

Solution

In Fig 11.7 (a),

$$I_1 = \frac{V_R}{2R} = \frac{10V}{2 \times 10 \times 10^3} = 0.5 \text{ mA}$$

$$I_2 = \frac{I_1}{2} = 0.25 \text{ mA}$$

and $$I_3 = \frac{I_2}{2} = 0.125 \text{ mA}$$

Therefore, current $$I_o = I_1 + I_2 + I_3$$

$$= 0.5 + 0.25 + 0.125 \text{ mA}$$

$$= 0.875 \text{ mA}$$

The output voltage, $$V_o = I_o \times R_f$$

$$= 0.875 \times 10^{-3} \times 10 \times 10^3$$

$$= 8.75 \text{ V}$$

11.2.4 Multiplying DACs

A digital to analog converter which uses a varying reference voltage V_R is called a multiplying D/A converter (MDAC). Thus if in the Eq. (11.1), the reference voltage v_R is a sine wave given by

$$v_R(t) = V_{im} \cos 2\pi ft$$

Then, $$v_o(t) = V_{om} \cos (2\pi ft + 180°)$$

where V_{om} will vary from 0V to $(1–2^{-n})\ V_{im}$ depending upon the input code. When used like this, MDAC behaves as a digitally controlled audio attenuator because the output V_o is a fraction of the voltage representing the input digital code and the attenuator setting can be controlled by digital logic. If followed by an op-amp integrator, the MDAC provides digitally programmable integration which can be used in the design of digitally programmable oscillators, filters.

11.2.5 Monolithic DAC : 1408 DAC

Monolithic DACs consisting of R-2R ladder, switches and the feedback resistor are available for 8, 10, 12, 14 and 16 bit resolution from various manufacturers. The MC 1408L is a 8-bit DAC with a current output. The SE/NE 5018 is also a 8-bit DAC but with a voltage output. There are hybrid D/A converters available in DATEL DAC-HZ series for current as well as voltage output.

A typical 8-bit DAC 1408 compatible with TTL and CMOS logic with settling time around 300 ns is shown in Fig. 11.8 (a). It has eight input data lines d_1 (MSB) through d_8 (LSB). It requires 2 mA reference current for full scale input and two power supplies V_{CC} = +5 V and V_{EE} – 5 V (V_{EE} can range from – 5 V to –15 V). The total reference current source is determined by resistor R_{14} and voltage reference V_R and is equal to V_R/R_{14} = 5 V/2.5 kΩ = 2 mA. The resistor $R_{15} = R_{14}$ match the input impedance of the reference source. The output current I_o is calculated as

$$I_o = \frac{V_R}{R_{14}} \left(\sum_{i=1}^{8} d_i\ 2^{-i} \right); d_i = 0 \text{ or } 1$$

For full scale input (i.e. d_8 through d_1 = 1)

$$I_o = \frac{5\text{ V}}{2.5\text{ k}\Omega} \left(\sum_{i=1}^{8} 1 \times 2^{-i} \right) = 2\text{ mA } (255/256) = 1.992\text{ mA}$$

The output is 1 LSB less than the full scale reference current of 2 mA. So, the output voltage V_o for the full scale input is

$$V_o = 2\text{ mA } (255/256) \times 5\text{ k}\Omega = 9.961\text{ V}$$

In general, the output voltage V_o is given by

$$V_o = \frac{V_R}{R_{14}} R_f \left[\frac{d_1}{2} + \frac{d_2}{4} + \frac{d_3}{8} + \ldots + \frac{d_8}{256} \right]$$

The 1408 DAC can be calibrated for bipolar range from –5 V to +5 V by adding resistor R_B (5 kΩ) between V_R and output pin 4 as shown in Fig. 11.8 (b). The resistor R_B supplies 1 mA (= V_R/R_B) current to the output in the opposite direction of the current generated by the input signal. Therefore the output current for the bipolar operation I_o' is

$$I_o' = I_o - (V_R/R_B) = (V_R/R_{14}) \left(\sum_{i=1}^{8} d_i 2^{-i} \right) - (V_R/R_B)$$

For binary input word = 00000000, i.e. zero input, the output becomes,

$$V_o = I_o' R_f = (I_o - V_R/R_B)R_f = (0 - 5\text{ V}/5\text{ k}\Omega) \times 5\text{ k}\Omega = -5\text{ V}$$

For binary input word = 10000000, output V_o becomes

$$V_o = (I_o - V_R/R_B)R_f = [(V_R/R_{14})\,(d_1/2) - (V_R/R_B)]R_f$$
$$= [(5\text{ V}/2.5\text{ k}\Omega)\,(1/2) - (5\text{ V}/5\text{ k}\Omega)]\,5\text{ k}\Omega = (1\text{ mA} - 1\text{ mA}) \times 5\text{ k}\Omega = 0\text{ V}$$

For binary input word = 11111111, output V_o becomes

$$V_o = [(V_R/R_{14})\,(255/256) - (V_R/R_B)]R_f = (1.992\text{ mA} - 1\text{ mA}) \times 5\text{ k}\Omega$$
$$= 0.992\text{ mA} \times 5\text{ k}\Omega = +4.960\text{ V}$$

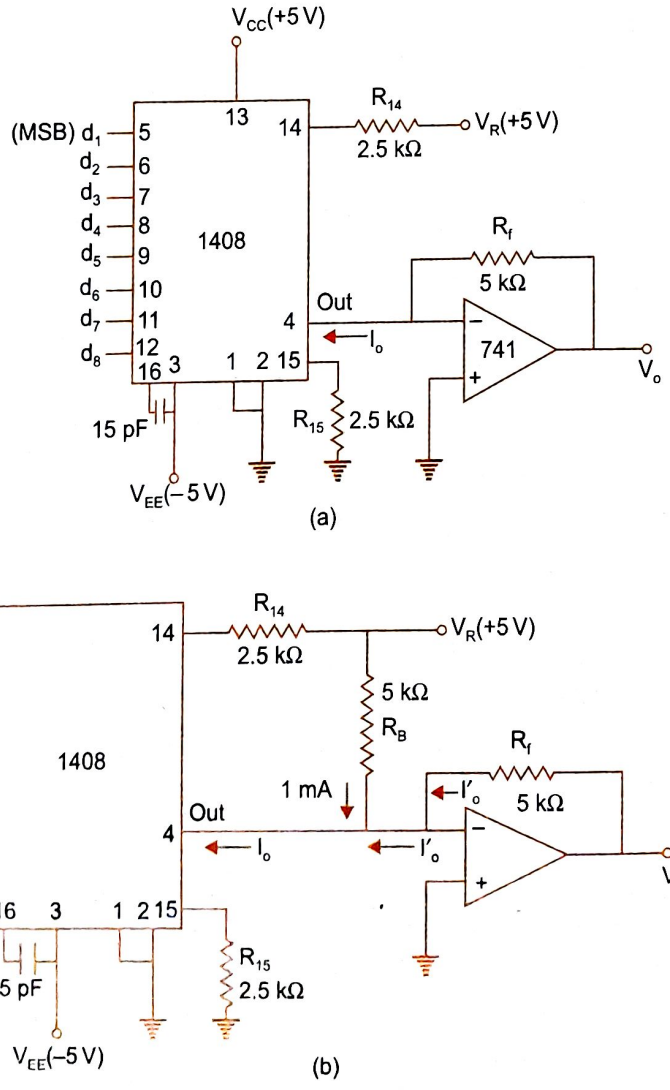


Fig. 11.8 1408 D/A converter (a) Voltage output in unipolar range (b) Modified circuit for bipolar output

Example 11.3

The basic step of a 9-bit DAC is 10.3 mV. If 000000000 represents 0 V, what output is produced if the input is 101101111?

Solution

The output voltage for input 101101111 is

$= 10.3 \text{ mV } (1 \times 2^8 + 0 \times 2^7 + 1 \times 2^6 + 1 \times 2^5 + 0 \times 2^4 + 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0)$

$= 10.3 \text{ mV } (367) = 3.78 \text{ V}$

Example 11.4

Calculate the values of the LSB, MSB and full scale output for an 8-bit DAC for the 0 to 10 V range.

Solution

$$\text{LSB} = \frac{1}{2^8} = \frac{1}{256}$$

For 10 V range, $$\text{LSB} = \frac{10 \text{ V}}{256} = 39 \text{ mV}$$

and $$\text{MSB} = \left(\frac{1}{2}\right) \text{ full scale} = 5 \text{ V}$$

Full scale output = (Full scale voltage – 1 LSB)

= 10 V – 0.039 V = 9.961 V

Example 11.5

What output voltage would be produced by a D/A converter whose output range is 0 to 10 V and whose input binary number is

(i) 10 (for a 2-bit D/A converter)
(ii) 0110 (for a 4-bit DAC)
(iii) 10111100 (for a 8-bit DAC)

Solution

(i) $V_0 = 10 \text{ V} \left(1 \times \frac{1}{2} + 0 \times \frac{1}{4}\right) = 5 \text{ V}$

(ii) $V_0 = 10 \text{ V} \left(0 \times \frac{1}{2} + 1 \times \frac{1}{2^2} + 1 \times \frac{1}{2^3} + 0 \times \frac{1}{2^4}\right)$

$= 10\left(\frac{1}{4} + \frac{1}{8}\right) = 3.75 \text{ V}$

(iii) $V_0 = 10 \text{ V } (1 \times 1/2 + 0 \times 1/2^2 + 1 \times 1/2^3 + 1 \times 1/2^4 + 1 \times 1/2^5$
$+ 1 \times 1/2^6 + 0 \times 1/2^7 + 0 \times 1/2^8)$
$= 10 \text{ V } (1/2 + 1/8 + 1/16 + 1/32 + 1/64) = 7.34 \text{ V}$

11.3 A-D CONVERTERS

The block schematic of ADC shown in Fig. 11.9 provides the function just opposite to that of a DAC. It accepts an analog input voltage V_a and produces an output binary word $d_1 d_2 ... d_n$ of

functional value D, so that

$$D = d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n} \qquad (11.3)$$

where d_1 is the most significant bit and d_n is the least significant bit. An ADC usually has two additional control lines: the START input to tell the ADC when to start the conversion and the EOC (end of conversion) output to announce when the conversion is complete. Depending upon the type of application, ADCs are designed for microprocessor interfacing or to directly drive LCD or LED displays.

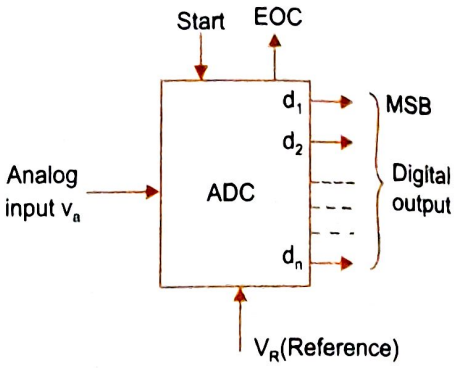


Fig. 11.9 Functional diagram of ADC

ADCs are classified broadly into two groups according to their conversion technique. Direct type ADCs and Integrating type ADCs. Direct type ADCs compare a given analog signal with the internally generated equivalent signal. This group includes

Flash (comparator) type converter
Counter type converter
Tracking or servo converter
Successive approximation type converter

Integrating type ADCs perform conversion in an indirect manner by first changing the analog input signal to a linear function of time or frequency and then to a digital code. The two most widely used integrating type converters are:

(i) Charge balancing ADC
(ii) Dual slope ADC

The most commonly used ADCs are successive approximation and the integrator type. The successive approximation ADCs are used in applications such as data loggers and instrumentation where conversion speed is important. The successive approximation and comparator type are faster but generally less accurate than integrating type converters. The flash (comparator) type is expensive for high degree of accuracy. The integrating type converter is used in applications such as digital meter, panel meter and monitoring systems where the conversion accuracy is critical.

DIRECT TYPE ADCs

11.3.1 The Parallel Comparator (Flash) A/D Converter

This is the simplest possible A/D converter. It is at the same time, the fastest and most expensive technique. Figure 11.10 (a) shows a 3-bit A/D converter. The circuit consists of a resistive divider network, 8 op-amp comparators and a 8-line to 3-line encoder (3-bit priority encoder). The comparator and its truth table is shown in Fig. 11.10 (b). A small amount of hysteresis is built into the comparator to resolve any problems that might occur if both inputs were of equal voltage as shown in the truth table. Coming back to Fig. 11.10 (a), at each node of the resistive divider, a comparison voltage is available. Since all the resistors are of equal value, the voltage levels available at the nodes are equally divided between the reference voltage V_R and the ground. The purpose of the circuit is to compare the analog input voltage V_a with each of the node voltages. The truth table for the flash type AD converter is shown in Fig. 11.10 (c). The circuit has the advantage of high speed as the

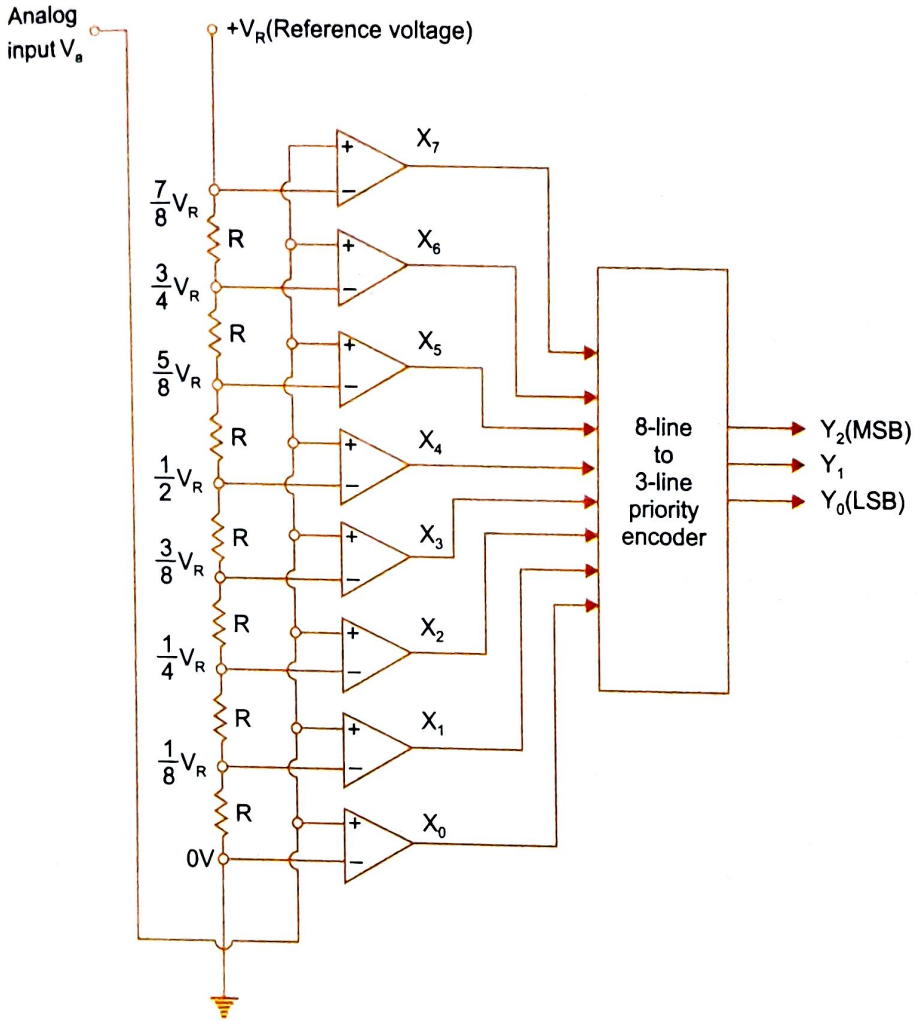


Fig. 11.10 (a) Basic circuit of a flash type A/D converter

Voltage input	*Logic output X*
$V_a > V_d$	$X = 1$
$V_a < V_d$	$X = 0$
$V_a = V_d$	Previous value

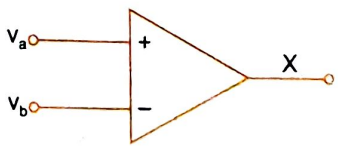


Fig. 11.10 (b) Comparator and its truth table

Input voltage V_a	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to $V_R/8$	0	0	0	0	0	0	0	1	0	0	0
$V_R/8$ to $V_R/4$	0	0	0	0	0	0	1	1	0	0	1
$V_R/4$ to 3 $V_R/8$	0	0	0	0	0	1	1	1	0	1	0
3 $V_R/8$ to $V_R/2$	0	0	0	0	1	1	1	1	0	1	1
$V_R/2$ to 5 $V_R/8$	0	0	0	1	1	1	1	1	1	0	0
5 $V_R/8$ to 3 $V_R/4$	0	0	1	1	1	1	1	1	1	0	1
3 $V_R/4$ to 7 $V_R/8$	0	1	1	1	1	1	1	1	1	1	0
7 $V_R/8$ to V_R	1	1	1	1	1	1	1	1	1	1	1

Fig. 11.10 (c) Truth table for a flash type A/D converter

conversion take place simultaneously rather than sequentially. Typical conversion time is 100 ns or less. Conversion time is limited only by the speed of the comparator and of the priority encoder. By using an Advanced Micro Devices AMD 686A comparator and a T1147 priority encoder, conversion delays of the order of 20 ns can be obtained.

This type of ADC has the disadvantage that the number of comparators required almost doubles for each added bit. A 2-bit ADC requires 3 comparators, 3-bit ADC needs 7, whereas 4-bit requires 15 comparators. In general, the number of comparators required are $2^n - 1$ where n is the desired number of bits. Hence the number of comparators approximately doubles for each added bit. Also the larger the value of n, the more complex is the priority encoder.

11.3.2 The Counter Type A/D Converter

The D to A converter can easily be turned around to provide the inverse function A to D conversion. The principle is to adjust the DAC's input code until the DAC's output comes within ± (1/2) LSB to the analog input V_a which is to be converted to binary digital form. Thus in addition to the DAC, we need suitable logic circuitry to perform the code search and a comparator of adequate quality to announce when the DAC output has come within ± (1/2) LSB to V_a.

A 3-bit counting ADC based upon the above principle is shown in Fig. 11.11 (a). The counter is reset to zero count by the reset pulse. Upon the release of RESET, the clock pulses are counted by the binary counter. These pulses go through the AND gate which is enabled by the voltage comparator high output. The number of pulses counted increase with time. The binary word representing this count is used as the input of a D/A converter whose output is a staircase of the type shown in Fig. 11.11 (b). The analog output V_d of DAC is compared to the analog input V_a by the comparator. If $V_a > V_d$, the output of the comparator becomes high and the AND gate is enabled to allow the transmission of the clock pulses to the counter. When $V_a < V_d$, the output of the comparator becomes low and the AND gate is disabled. This stops the counting at the time $V_a \leq V_d$ and the digital output of the counter represents the analog input voltage V_a. For a new value of analog input V_a, a second reset pulse is applied to clear the counter. Upon the end of the reset, the counting begins again as shown in Fig. 11.11 (b). The counter frequency must be low enough to give sufficient time

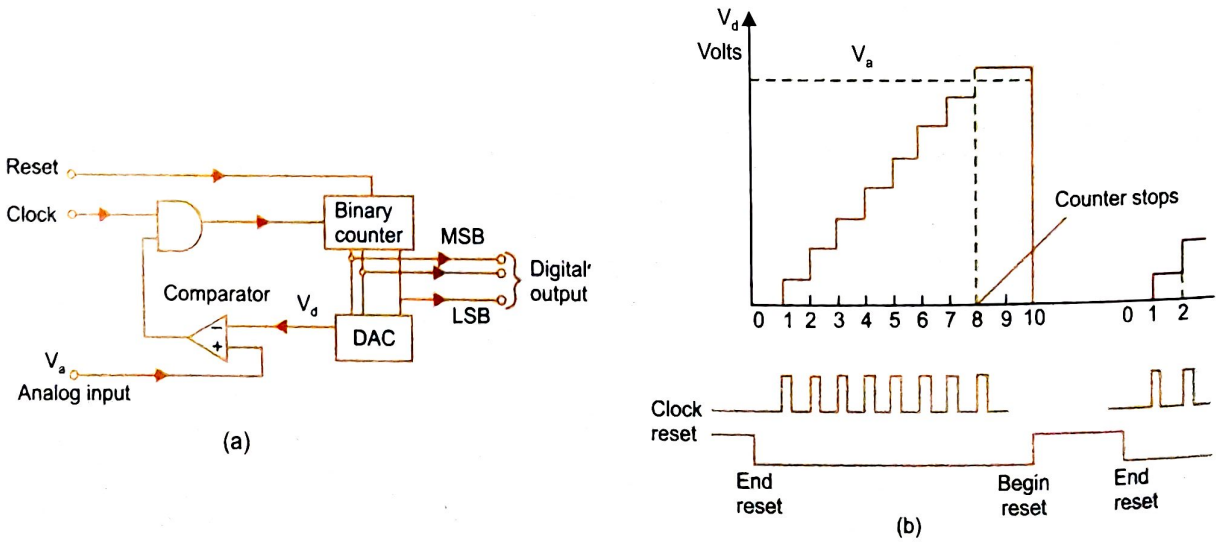


Fig. 11.11 (a) A counter type A/D converter, (b) D/A output staircase waveform

for the DAC to settle and for the comparator to respond. Low speed is the most serious drawback of this method. The conversion time can be as long as $(2^n - 1)$ clock periods depending upon the magnitude of input voltage V_a. For instance, a 12-bit system with 1 MHz clock frequency, the counter will take $(2^{12} - 1)$ μs = 4.095 ms to convert a full scale input.

If the analog input voltage varies with time, the input signal is sampled, using a sample and hold circuit before it is applied to the comparator. If the maximum value of the analog voltage is represented by n-pulses and if the clock period is T seconds, the minimum interval between samples is nT seconds.

11.3.3 Servo Tracking A/D Converter

An improved version of counting ADC is the tracking or a servo converter shown in Fig. 11.12 (a). The circuit consists of an up/down counter with the comparator controlling the direction of the count. The analog output of the DAC is V_d and is compared with the analog input V_a. If the input V_a is greater than the DAC output signal, the output of the comparator goes high and the counter is caused to count up. The DAC output increases with each incoming clock pulse and when it becomes more than V_a, the counter reverses the direction and counts down (but only by one count, LSB). This causes the control to count up and the count increases by 1 LSB. The process goes on being repeated and the digital output changes back and forth by ±1 LSB around the correct value. As long as the analog input changes slowly, the tracking A/D will be within one LSB of the correct value. However, when the analog input changes rapidly, the tracking A/D cannot keep up with the change and error occurs as shown in Fig. 11.12 (b).

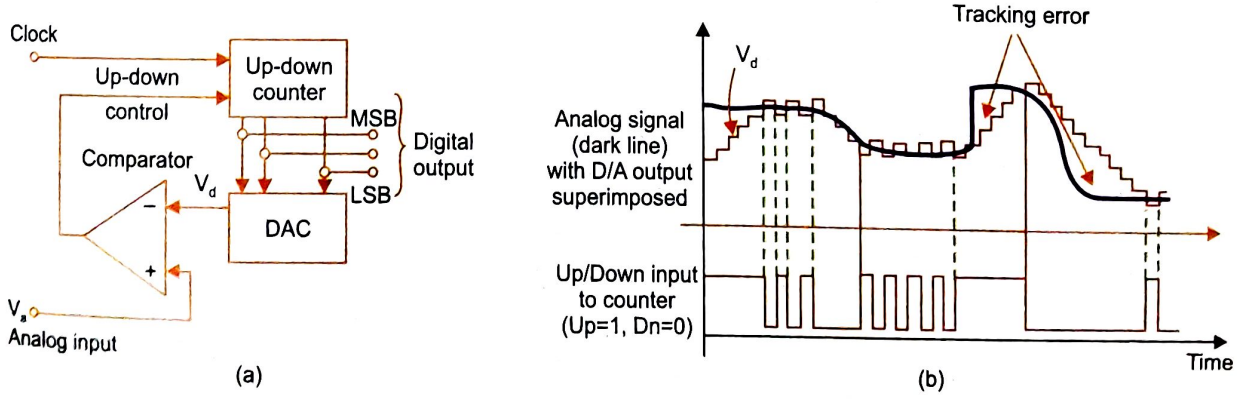


Fig. 11.12 (a) A tracking A/D converter, (b) Waveforms associated with a tracking A/D converter

The tracking ADC has the advantage of being simple. The disadvantage, however, is the time needed to stabilize as a new conversion value is directly proportional to the rate at which the analog signal changes.

11.3.4 Successive Approximation Converter

The successive approximation technique uses a very efficient code search strategy to complete n-bit conversion in just n-clock periods. An eight bit converter would require eight clock pulses to obtain a digital output. Figure 11.13 shows an eight bit converter. The circuit uses a

successive approximation register (SAR) to find the required value of each bit by trial and error. The circuit operates as follows. With the arrival of the START command, the SAR sets the MSB $d_1 = 1$ with all other bits to zero so that the trial code is 10000000. The output V_d of the DAC is now compared with analog input V_a. If V_a is greater than the DAC output V_d then 10000000 is less than the correct digital representation. The MSB is left at '1' and the next lower significant bit is made '1' and further tested.

However, if V_a is less than the DAC output, then 10000000 is greater than the correct digital representation. So reset MSB to '0' and go on to the next lower significant bit. This procedure is repeated for all subsequent bits, one at a time, until all bit positions have been tested. Whenever the DAC output crosses V_a, the comparator changes state and this can be taken as the **end of conversion** (EOC) command. Figure 11.14 (a) shows a typical conversion sequence and Fig. 11.14 (b).

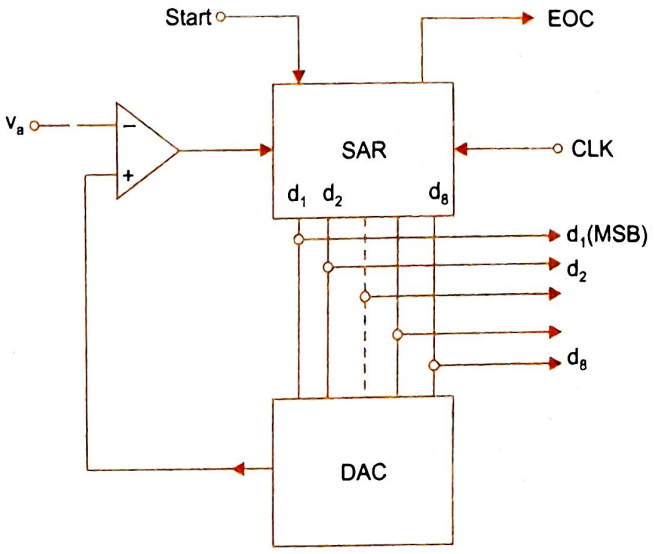


Fig. 11.13 Functional diagram of the successive approximation ADC

Correct digital representation	*Successive approximation register output V_d at different stages in conversion*	*Comparator output*
11010100	10000000	1 (initial output)
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0
	11010100	

Fig. 11.14 (a) Successive approximation conversion sequence for a typical analog input

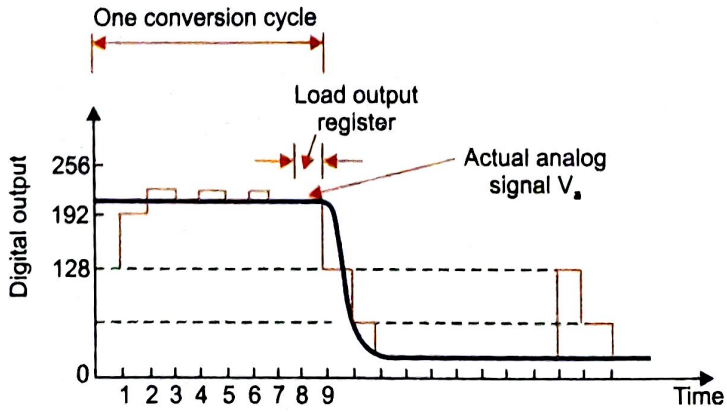


Fig. 11.14 (b) The D/A output voltage is seen to become successively closer to the actual analog input voltage

shows the associated wave forms. It can be seen that the D/A output voltage becomes successively closer to the actual analog input voltage. It requires eight pulses to establish the accurate output regardless of the value of the analog input. However, one additional clock pulse is used to load the output register and reinitialize the circuit.

A comparison of the speed of an eight bit tracking ADC and an eight bit successive approximation ADC is made in Fig. 11.15. Given the same clock frequency, we see that the tracking circuit is faster only for small changes in the input. In general, the successive approximation technique is more versatile and superior to all other circuits discussed so far.

Successive approximation ADCs are available as self contained ICs. The AD7592 (Analog Devices Co.) a 28-pin dual-in-line CMOS package is a 12-bit A/D converter using successive approximation technique.

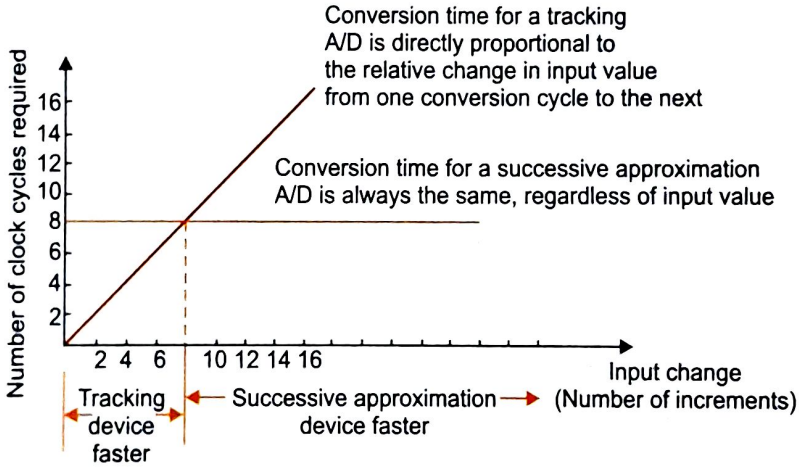


Fig. 11.15 Comparison of conversion times for tracking and successive approximation A/D devices

Example 11.6

An 8-bit A/D converter is used for converting 0 to 10V input voltage. Determine :

(i) input voltage required to change by 1 LSB

(ii) input voltage required to generate all 1's at the output

(iii) the digital output for an input voltage of 4.8V

Solution

(i) $1\ \text{LSB} = \dfrac{10V}{2^8} = 39.1\ \text{mV}$

(ii) Since digital output starts from 0 in a A/D converter, therefore the maximum full-scale input voltage will produce output less by 1 LSB for all digital output 1's.

Thus, $V_{FS} = 10V - 39.1\ \text{mV} = 9.961\ \text{V}$.

(iii) The digital output for an input voltage of 4.8V is given by

$$D = \frac{4.8V}{39.1mV} = 122.76$$

$$= 123$$

Converting this to binary gives the digital output as 01111011.

Example 11.7

The conversion rate of a 8-bit ADC is 9 μs. Find the maximum frequency of the input sine wave that can be digitized.

Solution

The maximum frequency is given by

$$f_{max} = \frac{1}{2\pi(T_C)2^n}$$

$$= \frac{1}{2\pi \times 9 \times 10^{-6} \times 2^8}$$

$$= 69.07 \text{ Hz.}$$

Integrating Type of ADCs

The integrating type of ADCs do not require a S/H circuit at the input. If the input changes during conversion, the ADC output code will be proportional to the value of the input averaged over the integration period.

11.3.5 Charge Balancing ADC

The principle of charge balancing ADC is to first convert the input signal to a frequency using a voltage to frequency (V/F) converter. This frequency is then measured by a counter and converted to an output code proportional to the analog input. The main advantage of these converters is that it is possible to transmit frequency even in noisy environment or in isolated form. However, the limitation of the circuit is that the output of V/F converter depends upon an RC product whose value cannot be easily maintained with temperature and time. The drawback of the charge balancing ADC is eliminated by the dual slope conversion.

11.3.6 Dual-Slope ADC

Figure 11.16 (a) shows the functional diagram of the dual-slope or dual-ramp converter. The analog part of the circuit consists of a high input impedance buffer A_1, precision integrator A_2 and a voltage comparator. The converter first integrates the analog input signal V_a for a fixed duration of 2^n clock periods as shown in Fig. 11.16 (b). Then it integrates an internal reference voltage V_R of opposite polarity until the integrator output is zero. The number N of clock cycles required to return the integrator to zero is proportional to the value of V_a averaged over the integration period. Hence N represents the desired output code. The circuit operates as follows:

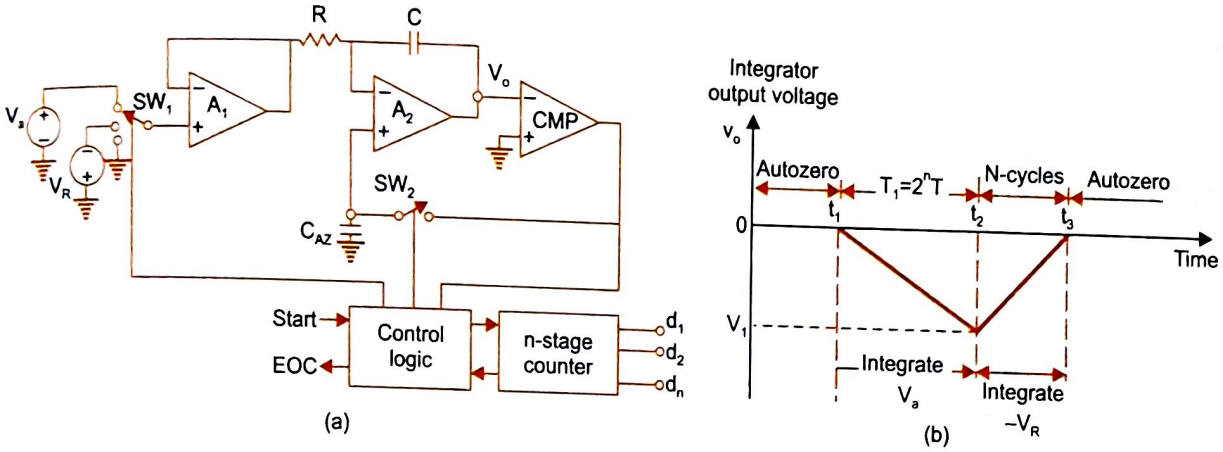


Fig. 11.16 (a) Functional diagram of the dual slope ADC (b) Integrated output waveform for the dual slope ADC

Before the START command arrives, the switch SW_1 is connected to ground and SW_2 is closed. Any offset voltage present in the A_1, A_2, comparator loop after integration, appears across the capacitor C_{AZ} till the threshold of the comparator is achieved. The capacitor C_{AZ} thus provides automatic compensation for the input-offset voltages of all the three amplifiers. Later, when SW_2 opens, C_{AZ} acts as a memory to hold the voltage required to keep the offset nulled. At the arrival of the START command at $t = t_1$, the control logic opens SW_2 and connects SW_1 to V_a and enables the counter starting from zero. The circuit uses an n-stage ripple counter and therefore the counter resets to zero after counting 2^n pulses. The analog voltage V_a is integrated for a fixed number 2^n counts of clock pulses after which the counter resets to zero. If the clock period is T, the integration takes place for a time $T_1 = 2^n \times T$ and the output is a ramp going downwards as shown in Fig. 11.16 (b).

The counter resets itself to zero at the end of the interval T_1 and the switch SW_1 is connected to the reference voltage ($-V_R$). The output voltage v_o will now have a positive slope. As long as v_o is negative, the output of the comparator is positive and the control logic allows the clock pulse to be counted. However, when v_o becomes just zero at time $t = t_3$, the control logic issues an end of conversion (EOC) command and no further clock pulses enter the counter. It can be shown that the reading of the counter at t_3 is proportional to the analog input voltage V_a.

In Fig. 11.16 (b)

$$T_1 = t_2 - t_1 = \frac{2^n \text{ counts}}{\text{clock rate}} \tag{11.4}$$

and

$$t_3 - t_2 = \frac{\text{digital count } N}{\text{clock rate}} \tag{11.5}$$

For an integrator,

$$\Delta v_o = (-1/RC)\, V(\Delta t) \tag{11.6}$$

The voltage v_o will be equal to v_1 at the instant t_2 and can be written as

$$v_1 = (-1/RC)\, V_a(t_2 - t_1)$$

The voltage v_1 is also given by

$$v_1 = (-1/RC)\, (-V_R)\, (t_2 - t_3)$$

So, $V_a(t_2 - t_1) = V_R(t_3 - t_2)$

Putting the values of $(t_2 - t_1) = 2^n$ and $(t_3 - t_2) = N$, we get

$$V_a(2^n) = (V_R)N$$

or, $$V_a = (V_R)\,(N/2^n) \tag{11.7}$$

The following important observations can be made:

1. Since V_R and n are constant, the analog voltage V_a is proportional to the count reading N and is independent of R, C and T.
2. The dual-slope ADC integrates the input signal for a fixed time, hence it provides excellent noise rejection of ac signals whose periods are integral multiples of the integration time T_1. Thus ac noise superimposed on the input signal such as 50 Hz power line pick-up will be averaged during the input integration time. So choose clock period T, so that 2^nT is an exact integral multiple of the line period (1/50) second = 20 ms.
3. The main disadvantage of the dual-slope ADC is the long conversion time. For instance, if $2^n - T = 1/50$ is used to reject line pick-up, the conversion time will be 20 ms.

Dual-slope converters are particularly suitable for accurate measurement of slowly varying signals, such as thermocouples and weighing scales. Dual-slope ADCs also form the basis of digital panel meters and multimeters.

Dual-slope converters are available in monolithic form and are available both in microprocessor compatible and in display oriented versions. The former provide the digital code in binary form whereas the display oriented versions present the output code in a format suitable for the direct drive of LED displays. The Datel Intersil ICL7109 is a monolithic 12-bit dual-slope ADC with microprocessor compatibility.

Example 11.8

A dual slope ADC uses a 16-bit counter and a 4 MHz clock rate. The maximum input voltage is +10 V. The maximum integrator output voltage should be – 8 V when the counter has cycled through 2^n counts. The capacitor used in the integrator is 0.1 μF. Find the value of the resistor R of the integrator.

Solution

Time period $(t_2 - t_1)$ in Fig. 11.16 (b) $= \dfrac{2^{16}}{4\text{ MHz}} = \dfrac{65536}{4\text{ MHz}} = 16.38\text{ ms}$

For the integrator

$$\Delta v_o = (-1/RC)\,V_a\,(t_2 - t_1)$$

So, $$RC = -(10\text{ V}/-8\text{ V})\ 16.3\text{ ms} = 20.47\text{ ms}$$

$$R = \frac{20.47\text{ ms}}{0.1\,\mu\text{F}} = 204.7\text{ k}\Omega = 205\text{ k}\Omega$$

Example 11.9

If the analog signal V_a is +4.129 V in the example 11.4, find the equivalent digital number.

Solution

Since, $V_a = V_R(N/2^n)$

So the digital count $N = 2^n\ (V_a/V_R) = 65536\ (4.129\text{ V}/8\text{ V}) = 33825$ for which the binary equivalent is 1000010000100001.

11.4 DAC/ADC SPECIFICATIONS

Both D/A and A/D converters are available with wide range of specifications. The various important specifications of converters generally specified by the manufacturers are analyzed.

Resolution: The resolution of a converter is the smallest change in voltage which may be produced at the output (or input) of the converter. For example, an 8-bit D/A converter has $2^8-1 = 255$ equal intervals. Hence the smallest change in output voltage is (1/255) of the full scale output range. In short, the resolution is the value of the LSB.

$$\text{Resolution (in volts)} = \frac{V_{FS}}{2^n - 1} = 1 \text{ LSB increment} \tag{11.8}$$

However, resolution is stated in a number of different ways. An 8-bit DAC is said to have
: 8 bit resolution
: a resolution of 0.392 of full-scale
: a resolution of 1 part in 255

Similarly, the resolution of an A/D converter is defined as the smallest change in analog input for a one bit change at the output. As an example, the input range of an 8-bit A/D converter is divided into 255 intervals. So the resolution for a 10 V input range is 39.22 mV (= 10 V/255). Table 11.1 gives the resolution for 6–16 bit DACs.

Table 11.1 Resolution for 6-16 bit DACs

Bits	*Intervals*	*LSB size (% of Full Scale)*	*LSB size (10 V Full Scale)*
6	63	1.588	158.8 mV
8	256	0.392	39.2 mV
10	1023	0.0978	9.78 mV
12	4095	0.0244	2.44 mV
14	16383	0.0061	0.61 mV
16	65535	0.0015	0.15 mV

Linearity: The linearity of an A/D or D/A converter is an important measure of its accuracy and tells us how close the converter output is to its ideal transfer characteristics. In an ideal DAC, equal increment in the digital input should produce equal increment in the analog output and the transfer curve should be linear. However, in an actual DAC, output voltages do not fall on a straight line because of gain and offset errors as shown by the solid line curve in Fig. 11.17. The static performance of a DAC is determined by fitting a straight line through the measured output points. The linearity error measures the deviation of the actual output from the fitted

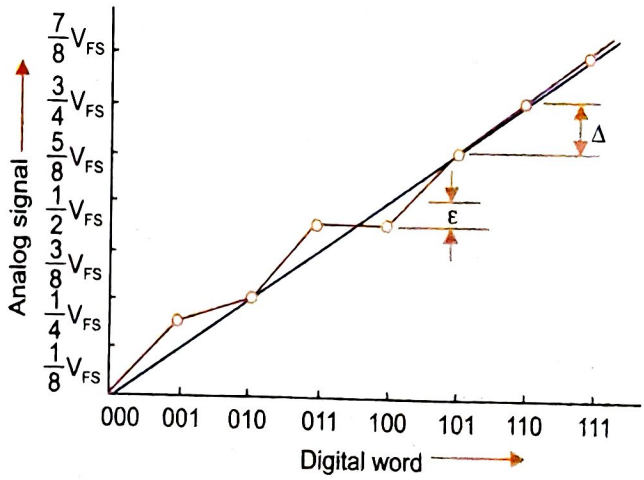


Fig. 11.17 Linearity error for 3-bit DAC

line and is given by ε/Δ as shown in Fig. 11.17. The error is usually expressed as a fraction of LSB increment or percentage of full-scale voltage. A good converter exhibits a linearity error of less than ± (1/2) LSB.

Accuracy: Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output. Relative accuracy is the maximum deviation after gain and offset errors have been removed. Data sheets normally specify relative accuracy rather than absolute accuracy. The accuracy of a converter is also specified in terms of LSB increments or percentage of full scale voltage.

Monotonicity: A monotonic DAC is the one whose analog output increases for an increase in digital input. Figure 11.18 represents the transfer curve for a non-monotonic DAC, since the output decreases when input code changes from 001 to 010. A monotonic characteristic is essential in control applications, otherwise oscillations can result. In successive approximation ADCs, a non-monotonic characteristic may lead to missing codes.

If a DAC has to be monotonic, the error should be less than ±(1/2) LSB at each output level. All the commercially available DACs are monotonic because the linearity error never exceeds ±(1/2) LSB at each output level.

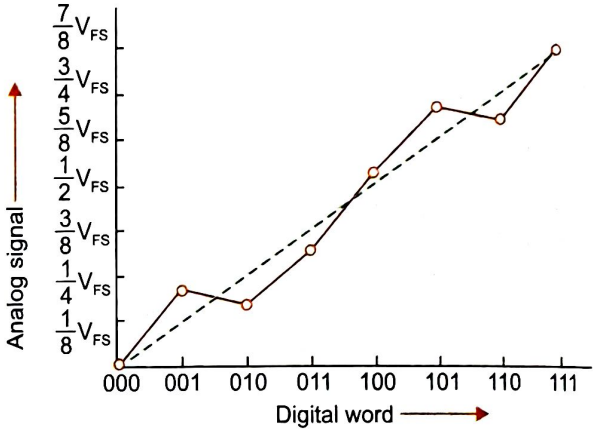


Fig. 11.18 A non-monotonic 3-bit DAC

Settling time: The most important dynamic parameter is the settling time. It represents the time it takes for the output to settle within a specified band ±(1/2) LSB of its final value following a code change at the input (usually a full scale change). It depends upon the switching time of the logic circuitry due to internal parasitic capacitances and inductances. Settling time ranges from 100 ns to 10 μs depending on word length and type of circuit used.

Stability: The performance of converter changes with temperature, age and power supply variations. So all the relevant parameters such as offset, gain, linearity error and monotonicity must be specified over the full temperature and power supply ranges.

A brief overview of ADC and DAC selection guide is given below:

A/D converters:	
AD 7520/AD 7530	10-bit binary multiplying type
AD 7521/AD 7531	12-bit binary multiplying type
ADC 0800/0801/0802	8-bit ADC
D/A converters:	
DAC 0800/0801/0802	8-bit DAC
DAC 0830/0831/0832	microprocessor compatible 8-bit DAC
DAC 1200/1201	12-bit DAC
DAC 1208/1209/1210	12-bit microprocessor compatible DAC

Example 11.10

We are familiar with 3½ digit digital voltmeter (DVM) and 4½ digit DVM which are being used regularly in the laboratory. Obviously 3½ digit DVM is less costly as its resolution is poor compared to 4½ digit DVM which is relatively costlier and have better resolution. Let us calculate the resolution of these DVMs.

Solution

In 3½ digit DVM, the MSB can be either 0 or 1 whereas the 3 digit LSBs can be 000 to 999. Hence in 3½ digit DVM, the reading variation can be from 0000 to 1999, that is 2000. The reference voltage is 2 V. Hence the resolution is (2/2000) V = 1 mV; that is voltage variation below 1 mV is not detectable. Similarly, in 4½ digit DVM the total variation is from 0 0000 to 1 9999 and reference voltage is 2 V. Hence the resolution is (2/20000) V = 0.1 mV. Thus, the resolution of a 4½ digit DVM is ten times better than that of 3½ digit DVM.

Example 11.11

Find the resolution and dynamic range of a D/A converter, if the maximum peak to peak output voltage is 5V and the input signal is a 10 bit word.

Solution

The 10-bit word represents $2^{10} = 1024$ levels. The step size is given by

$$= \frac{5V}{1024} = 4.88 \text{ mV}$$

Thus the system can identify input changes as low as 4.88 mv.

The dynamic range is the ratio of the largest value to the smallest value that can be converted. Therefore,

$$\text{Dynamic Range} = \frac{5V}{4.88\text{mv}}$$

$$= 1024$$

The dynamic range is usually given in dBs, so $20\log_{10}^{1024} = 60$ dB.

SUMMARY

1. The output of a DAC can be either a voltage or current.
2. A multiplying DAC is the one in which the analog signal is allowed to vary.
3. Three resistive techniques for D/A conversion are: weighted resistor DAC, R-2R ladder and inverter R-2R ladder.
4. DAC essentially requires: resistors, electronics switches and an op-amp.
5. Two types of digitally controlled SPDT electronic switches are in use: a totem-pole MOSFET driver, a CMOS inverter.
6. A weighted resistor DAC requires a wide range of resistor values for better resolution whereas a R-2R ladder type DAC requires only two values of resistors.

7. In an inverted R-2R ladder, the current through the resistors remains constant, irrespective of the input data. The constant node voltages therefore eliminate stray capacitance effect and improve circuit performance.
8. Monolithic DACs for 8, 10, 12, 14 and 16 bit resolution are available.
9. A/D converters are either direct type or indirect type. Most direct type ADCs require a D/A converter.
10. The important direct ADC techniques are: Parallel comparator (Flash), Counting type, Tracking type and Successive approximation technique.
11. Integrating type ADCs perform conversion in an indirect manner. The two important converters are: Charge balancing ADC, Dual slope ADC.
12. The parallel comparator ADC is the fastest technique. But it has the disadvantage of using maximum hardware. A counting type A/D converter has low speed with conversion time as long as $(2^n - 1)$ clock periods for n-bit ADC. A tracking ADC is simple but gives error when analog signal changes rapidly.
13. Successive approximation type ADC is the most versatile. It completes n-bit conversion in just n-clock periods. Most monolithic ADCs are successive approximation type.
14. Dual slope converters are suitable for precise measurement of slowly varying signals. All digital voltmeters use dual-slope ADC. The disadvantage is of long conversion time.
15. Monolithic dual slope ADCs are available in microprocessor compatible and display-oriented versions.
16. The important converter characteristics are: Resolution, Linearity, Accuracy, Monotonicity, Settling time, Stability etc.

REVIEW QUESTIONS

11.1. Classify DACs on the basis of their output.
11.2. Name the essential parts of a DAC.
11.3. Describe the various types of electronic switches used in D/A converter.
11.4. How many resistors are required in a 12-bit weighted resistor DAC?
11.5. Why is an inverted R-2R ladder network DAC better than R-2R ladder DAC?
11.6. List the various A/D conversion techniques.
11.7. Which is the fastest ADC and why?
11.8. Give the conversion time for (i) counting ADC (ii) successive approximation ADC (iii) dual-slope ADC.
11.9. Explain the operation of Dual-slope ADC.
11.10. Explain how Dual-slope ADC provides noise rejection.
11.11. Explain the important specifications of D/A and A/D converters.

PROBLEMS

11.1. How many levels are possible in a two-bit DAC? What is its resolution if the output range is 0 to 3 V?

11.2. A 5-bit D/A converter is available. Assume that '00000' corresponds to an output of +10 V and that the D/A converter is connected for – 0.1 V per increment, what output voltage will be produced for '11111'?

11.3. If a 10-bit D/A converter spans a range of 0 to 10 V and is always within 1 mV of its ideal output. What is its linearity as a per cent of full-scale range?

11.4. Find the voltage at all nodes 0, 1, 2, ... and at the output of a 5-bit R-2R ladder DAC. The least significant bit is 1 and all other bits are equal to 0. Assume $V_R = -10$ V and $R = 10$ kΩ.

11.5. The Fig. P. 11.5 shows a binary weighted resistor D/A converter.

(i) Show that the output resistance is independent of the digital word and that

$$R_o = \frac{2^{N-1}}{2^N - 1} R$$

(ii) Show that the analog output voltage for the MSB is

$$V_o = \frac{2^{N-1}}{2^N - 1} V_R$$

(iii) Show that the analog output voltage for the LSB is

$$V_o = \frac{1}{2^N - 1} V_R$$

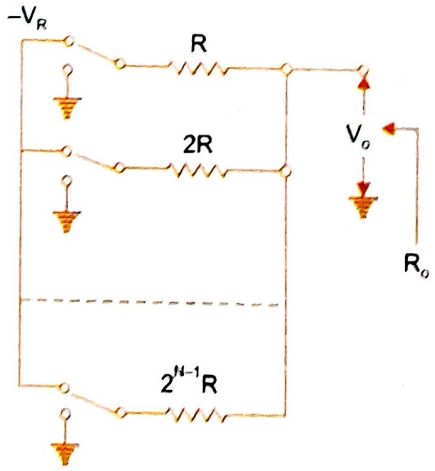


Fig. P. 11.5

11.6. (a) Draw the circuit diagram of a 6-bit inverted R-2R ladder DAC.

(b) For $V(1) = 5$ V, what is the maximum output voltage?

(c) What is the minimum voltage that can be resolved?

11.7. The analog input signal ranges for –5 to +8 V in a nine bit A/D converter.

(i) How many quantization levels are available with this A/D converter?

(ii) What is the resolution in volt per increment?

(iii) What binary number will be produced when the analog input is zero volt?

11.8. A counting A/D converter uses a 7-bit DAC. The MSB of DAC output voltage is +5 V.

(i) If the analog input voltage is +6.85 V, what will be the R-2R ladder output voltage when the clock stops?

(ii) What is the number of clock pulses that occur between the release of reset and stopping of the clock?

11.9. The ADC in problem 11.8 uses a 100 kHz clock. How long did it take to digitize 6.85 V?

11.10. What is the conversion time of a 10-bit successive approximation A/D converter if its input clock is 5 MHz?

11.11. A dual slope ADC uses a 18-bit counter with a 5 MHz clock. The maximum input voltage is +12 V and the maximum integrator output voltage at 2^N count is – 10 V. If R = 100 kΩ, find the size of the capacitor to be used for integrator.

11.12. The dual slope ADC of problem 11.11 has an input voltage of +5.237 V. Determine the digital number in binary which represents the count in the register.

EXPERIMENT 11.1

To construct a 4-bit R-2R ladder type D/A converter. Plot the transfer characteristics, that is, binary input vs output voltage. Calculate the resolution and linearity of the converter from the graph.

(i) Choose R = 10 kΩ, $2R$ = 20 kΩ of tolerance ±1% or less.

(ii) For logic '0' short to ground and logic '1' connect to a +5 V supply.

PROCEDURE

1. Set-up the circuit shown in Fig. E. 11.1.
2. With all inputs (d_0 to d_3) shorted to ground, adjust the 20 kΩ-pot until the output is 0 V. This will nullify any offset voltage at the input of the op-amp.

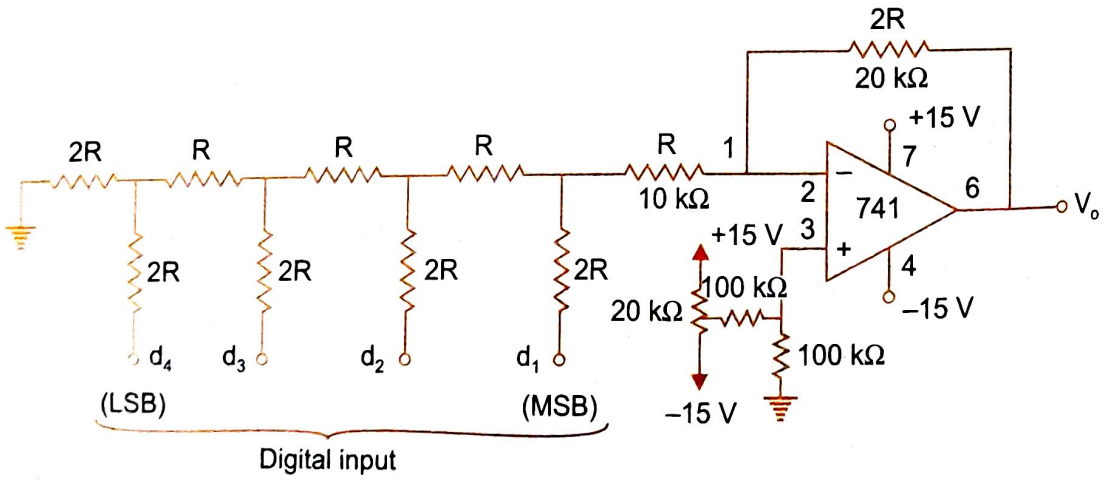


Fig. E. 11.1 A 4-bit R-2R ladder D/A converter